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Introduction

With the introduction of the European WEEE (Waste in Electrical and Electronic Equipment) Directive in 2006, which aims to raise the level of recycling of electrical and electronic equipment (EEE) and encourages designers to create products with recycling in mind, there is great interest in any potential low temperature manufacturing route for electronics that would enable the use of materials that are easy to disassemble/ separate and recycle. Such routes could increase the potential recyclable content of electronics assemblies enabling a significant reduction in amount of electronics waste entering landfills. It was recently estimated in a DTI-funded report, that around 85% of all PCB scrap board waste goes to landfill, with around 70% of this being of non-metallic content (primarily reinforced epoxy substrate material) with little opportunity for recycling. Based on 1998 estimates, non-recyclable substrate materials contribute around 3.5 million tonnes or over 2% of the municipal waste stream annually and the growth in this waste stream is currently three times higher than the average municipal waste.

A potential route to enable higher levels of recycling in electronics assemblies is to use low temperature curing electrically conductive polymer adhesives (CAs) in conjunction with low cost recyclable substrates. Thermoplastic substrates can be fabricated by electroless plating of the plastic, followed by imaging, electroplating and etching. Conventional electroless surface finishes such as ENIG (electroless nickel/immersion gold) and immersion Ag can be applied. Such subtractive substrates (additional material is added and then removed during their manufacture) have the advantage of being able to be fabricated using the existing PCB fabrication industry infrastructure.

The adhesives used are generally silver filled epoxy systems, with isotropic electrical properties, which can be applied and cured using the same equipment required for solder paste printing and reflow. There is no current test method for assessing the reliability of such systems, which differ in fundamental construction from the traditional solder/epoxy/glass constructions typical of electronics today. The failure modes for these novel ‘solder and glass free’ systems are very different from those experienced with conventional solder joints.

This Note describes a new combinational method for the measurement of relative reliability of isotropic conductive adhesive (ICA) assemblies. Previous work at NPL (References 1 to 3) has indicated that thermal cycling, the conventional methods of reliability assessment for soldered assemblies, is not the best method for stressing ICA joints. This is because these materials are compliant and thus deform to take up the thermal coefficient of expansion (TCE) mismatches between components and PCBs. Prolonged exposure to damp heat causes a more significant degradation in conductive performance of ICA joints. Whilst the conductivity of the bulk material is generally unaffected by the damp heat conditioning because any silver oxide formed is still electrically conductive, the conditioning affects the conductivity of the surface finishes of the component terminations and PCB pads, due to the formation of oxides which are not conducting. The damp heat may also have the effect of reducing the adhesive bond between the epoxy based adhesive and the component and PCB terminations. It should be noted that thermoplastic substrates generally have a higher TCE than their conventional glass fibre reinforced equivalents.

2 Test Procedures

The test procedure to generate the required reliability data is essentially straight forward, using a combination of thermal cycling and damp heat conditioning. By using low value resistors and daisy chained components, the electrical resistance of circuits is monitored periodically during conditioning until significant resistance changes are noted.

3 Test Requirements

Test Equipment: the required testing regime to undertake the reliability evaluation must have three attributes. An oven capable of maintaining a damp atmosphere of 85^{o}C/85%RH; a thermal cycling oven capable of changing the temperature of the test assemblies between –55^{o}C and 125^{o}C with a 5 minute dwell at each extreme and a maximum rate of change between extremes of not greater than 10^{o}C per minute. Finally, a means of monitoring the electrical resistance of conductive chains within the test assembly is required.

Test Specimen: a purpose-designed test circuit is required incorporating the component styles required to be evaluated. An example of the component side of a double-sided circuit is shown in Figure 1, which incorporates 1206 and 0603 resistors and SOIC14 components. These components have been chosen as the chip resistors have a large TCE mismatch with the substrate and are normally terminated with a tin plated finish, which oxidises to increase joint resistance. The SOIC represent a different joint configuration which can prove problematic with conductive adhesives and is also representative of a typical solder terminated component. For ease of measurement all the individual circuits are led out to test points at the left hand end of the assembly. Alternatively, an actual working circuit could be evaluated, providing that the circuit performance would be effected by joint resistance increases and that this could be periodically monitored during conditioning. The test circuit below also includes vias to evaluate z-axis expansion effects on via reliability. Test circuits should include at least 30 test circuits. Multiple assemblies may be used to achieve this.

4 Test Method

To determine relative reliability of conductively joined electronics assemblies, it is recommended that the assemblies be first subjected to 500 thermal cycles between –55^{o}C and 125^{o}C with a 5 minute dwell at each extreme and a maximum rate of change between extremes of not greater than 10^{o}C per minute. If the glass transition temperature (Tg) of the thermoplastic used is below the upper thermal cycling temperature, care must be taken to ensure

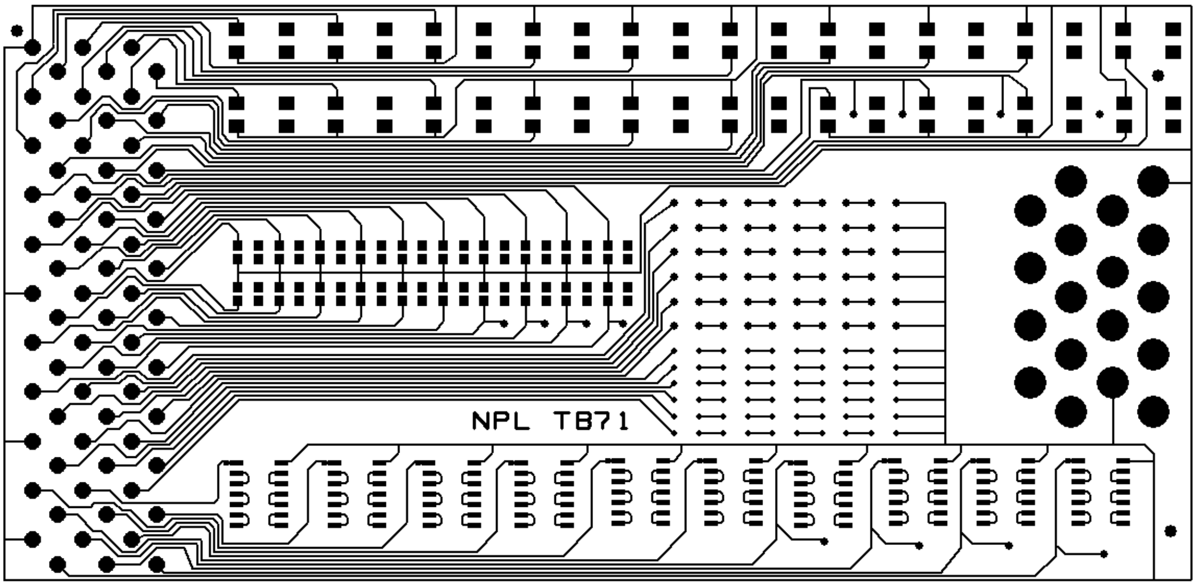

Figure 1: Example test circuit for reliability testing

that the substrates do not deform during thermal cycling. If the Tg is low, it is recommended that the substrates be mounted horizontal and supported over their entire area during thermal cycling. For higher Tg substrates vertical mounting during thermal cycling is permissible. The electrical resistance of test circuits should be monitored and recorded before and after thermal cycling at room temperature. Ideally circuit resistances should be less than 20Ω at the start of thermal cycling. The thermal cycling is then followed by at least 500 hours of damp heat conditioning at 85°C/85%RH. Electrical resistance monitoring should be undertaken at room temperature at least every 250 hours until a 50% failure level is reached. Failure criteria may be set by the end user, but a resistance increase to 100Ω has been used successfully applied at the National Physical Laboratory as a failure level. This combinational testing creates significantly earlier failures than either damp heat or thermal cycle testing alone. This is indicated in Figures 2 and 3, where NPL data on identical assemblies clearly shows earlier failures for both 1206 resistors (two different ICAs, P & X) and SOICs, when tested by combinational testing compared to just damp heat or thermal cycling. Figure 4 shows a comparison of the shear strengths of the R1206 components after damp heat, thermal cycling and combinational testing for 1000 cycles or hours. The thermal cycling followed by damp heat shows a greater fall in shear strength than for the other test methods. It should also be noted that the thermal cycling should be undertaken before damp heat testing not in the reverse order. This latter combination does not generate failures any faster than just damp heat conditioning or thermal cycling alone. By subjecting the assembly initially to thermal cycling an interfacial breakdown is accelerated, driven by the TCE mismatch between the components and the substrate or the components/substrates and the adhesive. Following this with damp heat conditioning ensures oxides form more quickly on the exposed surfaces of the conductors.

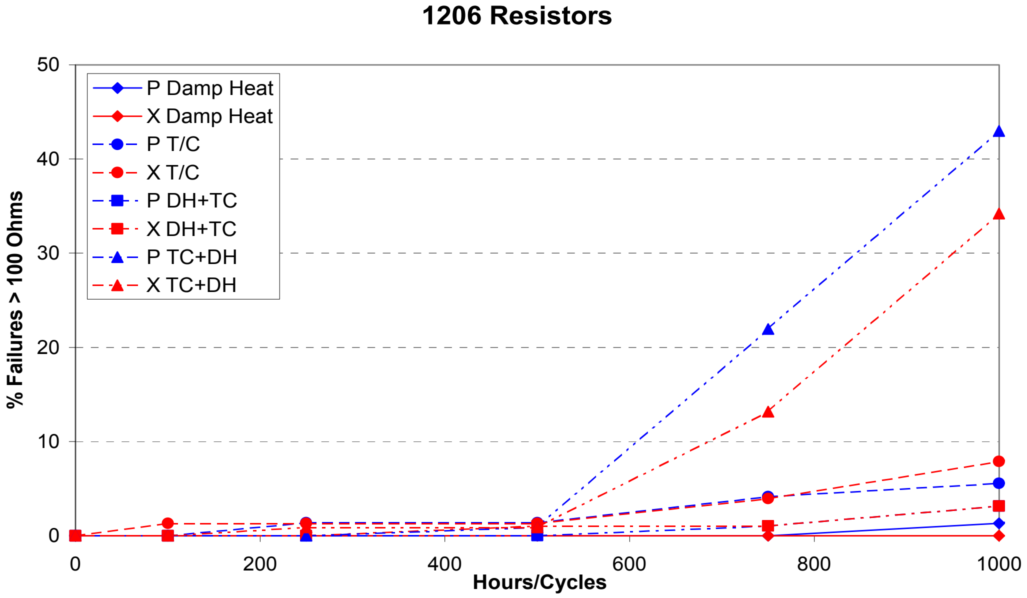

Figure 2: Comparison of damp heat, thermal cycling, damp heat + thermal cycling and thermal cycling + damp heat testing for two ICAs (P & X) for 1206 resistors

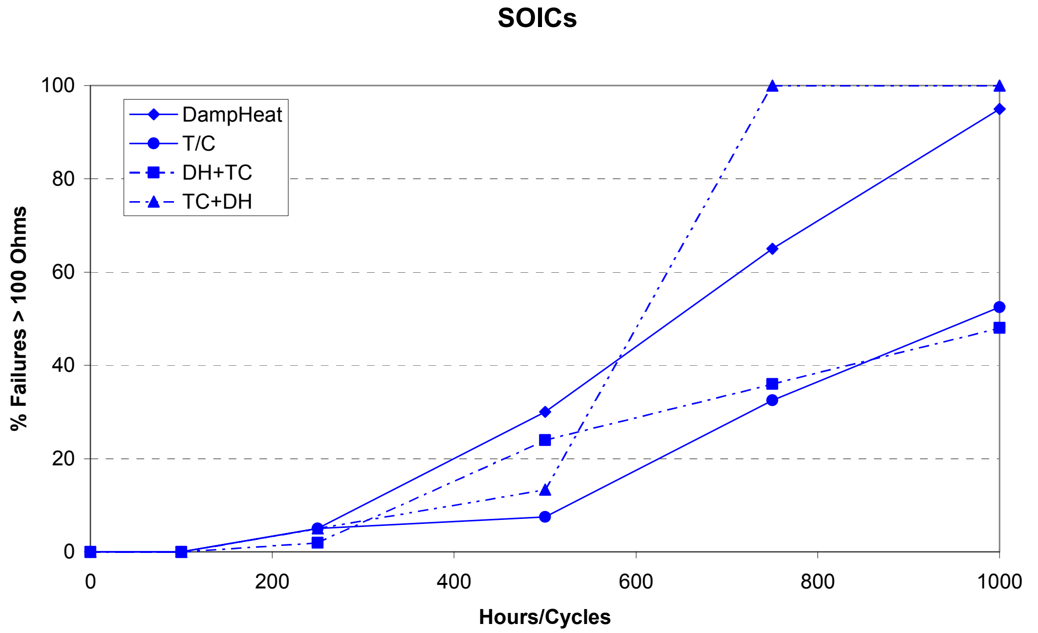

Figure 3: Comparison of damp heat, thermal cycling, damp heat + thermal cycling and thermal cycling + damp heat testing for SOICs

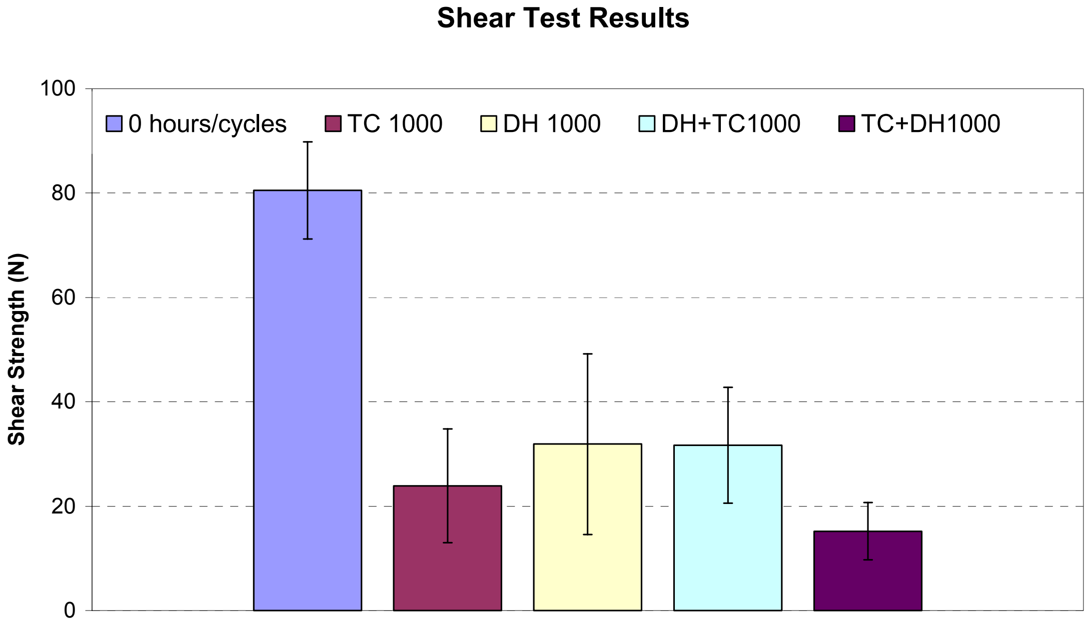

Figure 4: Comparison of average shear strengths of R1206 ICA joints conditioned using damp heat, thermal cycling, damp heat + thermal cycling and thermal cycling + damp heat

Acknowledgements

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References

1. Wickham, M, Zou, L, Hunt, C P; Measuring the reliability of technology demonstrator manufactured with isotropic electrically conductive adhesives; NPL Report DEPC-MPR 046, December 2006
2. Wickham, M, Zou, L, Hunt, C; Measuring the effect on isotropic electrically conductive adhesive reliability of substrate and component finishes; NPL Report DEPC-MPR 031, August 2005
3. Wickham, M, Zou, L, Hunt, C; Developing a stress screening regime for isotropic electrically conductive adhesives; NPL Report DEPC-MPR 005, July 2004

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