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DEPC-MN 001

Measurement Note - Crack Detection Methods For Lead-free Solder Joints

ABSTRACT

This Note describes the suitability of a number of techniques of potential use in studying cracking in lead-free solder joints, and hence their use in assessing joint lifetimes. Cracks induced into solder joints of chip resistors on FR4 substrates, were studied using micro-sectioning, dye penetration, mechanical test and thermal conductivity techniques. The work previously reported [1] has been used as the basis for comments, especially regarding understanding of the tests themselves. The work has shown that those techniques traditionally used to study lead-based solder joints can be used for assessing lead-free solder joints. Although micro-sectioning is suitable for locating and imaging joint cracking, especially when the section is examined in a SEM, it is not very suitable for quantitative analysis of cracks or their detection in small components. Dye penetration techniques allow a better characterisation of cracks in the horizontal plane and can provide a quantitative measure of the cracked surface area. Shear testing is a proven method [2] for evaluating not only the degree of crack propagation and damage to the solder joint, but also the general strength of the joint. The other methods considered (3 and 4-point bend tests, pull test and heat transfer) have severe limitations and are unsuitable for studying cracks in electronics solder joints.

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no significant difference in the temperature distribution in the joints of the components over the heating up period. The only significant changes occurred when the length of the crack exceeded 72% of the termination length. But it is probable that cracks of this scale would already have caused the joint to fail mechanically. In consequence, this technique cannot be recommended for the assessment of crack initiation and propagation in solder joints.

1. Introduction.

In electronics assemblies components and substrates are mechanically and electrically interconnected via soldering processes, and since the solder joint is the weakest point in the assembly, it usually determines the lifetime of the assembly. Hence estimates of the lifetime of electronics assemblies are often made by monitoring the degradation (and eventual failure) of solder joints under severe service or accelerated conditions. Such estimations of the joint lifetimes are also desirable, if not necessary, for feedback to achieve and maintain good process control, especially for high reliability applications.

In normal field use these assemblies experience a variety of temperature/power changes (e.g. power consumption; switching equipment on/off; day/night temperature changes), and these TCE mismatches cause strain and stress in solder joints, which creep and relax over time. Such strains can result in crack initiation (usually in the solder joint under the component), subsequent crack propagation through the solder fillet itself, and finally failure of the joint. There are several investigatory techniques which are used to study cracking in conventional SnPb solder joints, and which are therefore potentially suitable for providing data on the lifetime of lead-free solder joints. Previous work [3] on mechanical studies of solder joints has demonstrated that mechanical failure of the joint does not happen in a sudden, catastrophic manner, but occurs as a gradual change, usually in the form of cracking.

This Measurement Note provides an assessment of the suitability of a number of techniques to study cracking in lead-free solder joints, and hence their use in estimating joint lifetimes. The techniques described, which were selected as those commonly used (or being evaluated) in the electronics manufacturing industry, were metallographic micro-sectioning, dye penetration, mechanical tests and thermal conductivity. Where appropriate, suitable test procedures are detailed, and the previous work [1] has been used as the basis for the comments concerning the suitability of the technique studied.

2. Test Procedures

The test procedure is essentially simple using devices mounted on a test board, which is subjected to a thermal cycling regime in order to accumulate damage in the joints in the form of cracking. The devices used are known to provide sensitive joints when soldered, and hence to be susceptible to cracking. Resulting cracks are then sought and characterised using the various evaluation techniques.

Components : R2512-type chip resistors – chosen as frequently used, sensitive structures, most likely to fail first in the field due to high CTE mismatches (see Figure 1), and which also lend themselves to shear tests. The terminations should contain no lead, since small additions of lead are known to alter solder properties such as alloy strength [2].

Substrate Finish : FR4 substrates with the ENIG (immersion gold over electroless nickel) finish - they are lead-free, in common usage and widely available.

Test Assembly Design : an example of a suitable PCB layout for testing is shown in Figure 1. The board is single-sided FR4, thickness 1.6 mm, copper thickness of 35 µm (copper plating 1 oz/sq.ft) and an ENIG finish.

Board Assembly : substrates should be printed with solder paste using a stainless steel stencil with a thickness of 150 µm (0.006”). Two pastes have been found suitable and give broadly similar results [2] for the cycling regime described here i.e. SAC (95.5Sn3.8Ag0.7Cu) and

96.5Sn3.5Ag. An automatic placement system is more likely to provide consistent solder volumes for each joint, and convection reflow assembly is preferred. Reflow temperature profiles should be measured [2] to ensure that the times above 220^{O}C and 250^{O}C are not excessive.

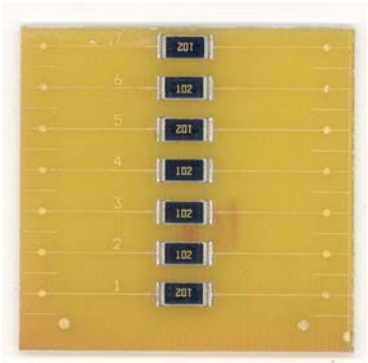

Figure 1. FR4 laminate with 2512-type resistors used in the crack assessment study.

Cycling Regime : The traditional accelerated method of generating cracks in solder joints is to subject the assemblies [4] to thermal cycling regimes, during which the cracks are caused by stresses exceeding the ultimate shear stress of the particular solder alloy. The localised stresses can be caused mechanically, by material displacement, or by mismatch of the coefficients of thermal expansion (CTE) of the two joined materials exposed to temperature changes.

In many electronic assemblies typical mismatches in CTE are between the component body (alumina 6.5ppm/°C), the solder (21-25ppm/°C), the copper termination pad (17.6ppm/°C) and the FR4 laminate (CTE_{xy} = 12-18ppm/°C, CTE_z = 50ppm/°C). An additional factor is that all these coefficients vary with temperature. The largest mismatch over the longest absolute dimension is between the component body and the FR4 substrate [5]. The parameters of the thermal cycling regime now commonly used are listed in Table 1.

Table 1: Tested temperature cycling regimes within ± 4°C of the set value

Cycle	Low temp	High temp	Ramp	Dwell	Period
	[°C]	[°C]	[°C/min]	min	min
A	-55	125	10	5	45

This is the test regime commonly used for military applications – hence it has a wide temperature cycle (-55 to +125^{O}C). The ramp rate of 10°C/min is moderate, but slower than that of a thermal shock regime, which is typically above 30°C/min [4]. The relatively short dwell time of 5 minutes is to minimize the cycle period and shorten the overall test time. In recent years the military and automotive sectors have preferred to use the same cycling regime, and this now appears suitable for many, if not all, applications. It not only reflects a severe working environment, but also provides a means of rapid damage (e.g. crack) accumulation without compromising the failure modes.

is such that the gap between the unbending lower face of the resistor and the board itself is closed and contact may occur. This issue, together with those associated with the attachment of strain gauges, means this test approach cannot be recommended for assessing cracking or solder joint lifetime until further development has been carried out.

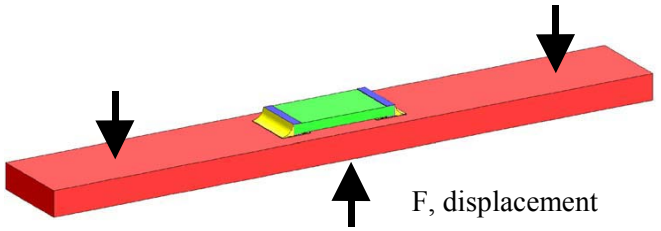

Figure 6. Schematic of the 3-point bend test.

5.4. 4-Point Bent Test

The 4-point bend test is an alternative method to the 3-point bend test, the major difference being that the solder joints are stressed in the opposite direction to that used in the 3-point test. Figure 7 illustrates the layout and the direction of the forces acting at the assembly. However, this testing method cannot be recommended [1] since it is inherently unsuitable for crack assessment - the test itself results in propagation of the cracks, a consequential peeling of the remaining solder joint, and early and anomalous joint failure.

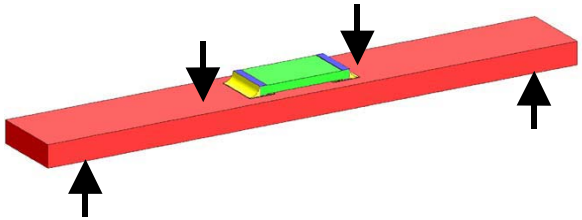

Figure 7. Test specimen with forces (arrows) acting in 4-point bend test.

6. Thermal Conductivity

It has been suggested that cracks inside the solder joint might affect its thermal conductivity, because as the crack develops the direct conduction path in the material becomes less, resulting in a decrease in the rate of heat transfer [7]. Modelling this situation using FEA techniques, however, confirmed [1] the unsuitability of the technique in characterising cracks and crack propagation. The results highlighted that almost irrespective of the size of the crack there was

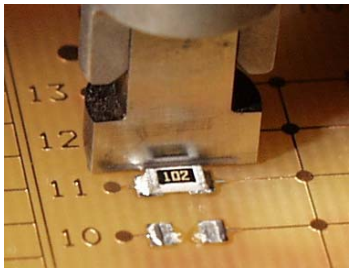

Figure 4. Shear test jig and push-off tool before a shear test.

5.2. Pull Test

In another destructive mechanical test, the pull test (see Figure 5), a constant force is applied to the joint and the deformation measured using a strain gauge mounted on the top of a resistor. Typical parameters [1] might be a load of 100N applied over 20 sec at a rate of 3.3 N/sec and held for 60 sec.

The previous work [1] demonstrated that this technique is still in its development stages and hence can produce unexpected and variable results. The latter may be operator-dependent and associated with factors such as the alignment of specimen, the bonding of the strain gauge, and/or the small resistor area. Importantly, however, the method cannot currently be recommended for the assessment of solder joint integrity because of the complications arising from the strain gauge attachment. Better results might be achieved [7] using a field strain monitoring using moiré technique.

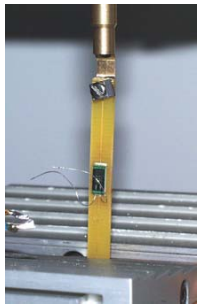

Figure 5. Specimen for pull testing.

5.3. 3-Point Bend Test

In the 3-point bend test the force is applied to the substrate on the side opposite to that of the resistor (see Figures 6), and the substrate deformation is monitored at the top of the resistor body. The extent of the deformation depends on the force exerted on the resistor through the solder joint. The previous work [1] demonstrated that irrespective of the thermal cycling regime used, the solder becomes accommodating and irreversible plastic deformation (creep) occurs in the joints during the dwell periods of the test. In consequence the curvature of the bending board

3. Micro-sectioning

Metallographic micro-sectioning is the traditional destructive method of studying microstructure and failure modes in solder joints, including the location and extent of any cracking within the solder joint (see Figure 2). However, for credible evaluations of cracking it is essential that microsections be carefully prepared, and there are some general points which can be highlighted:

- assemblies of component and substrates should be pre-cut using a low speed saw to avoid causing any additional stressing
- these pre-cut specimens should be mounted in cold curing epoxy resin moulds to protect and encapsulate the solder joints
- the specimens should be ground using successive grades of silicon carbide papers (120 to 4000 grit), followed by polishing using diamond pastes/sprays with successive particle sizes from 15 to 0.25 µm in diameter
- due to the differences in hardness of the solder, the copper pad, any interlayer present, and the component edge, care should be exercised to ensure that only a light pressure is used during polishing
- diamond impregnation of the polishing cloth should be kept to a maximum to ensure an optimum cutting rate. Final polishing of the samples should be carried out by hand using a gamma aluminide powder suspended in lapping fluid (OP-S)
- etching of *lead-based solder joints* to highlight microstructure, should be carried out using a solution containing 2 ml hydrochloric acid and 98 ml industrial methylated spirits in a polish-etch technique, employing 0.25µm diamond paste as the polishing medium
- etching of *lead-free solder joints* to highlight microstructure, should be carried out using a solution containing 2 ml nitric acid, 2 ml hydrochloric acid and 96 ml distilled water in a polish-etch technique, with 0.25µm diamond paste as the polishing medium. Satisfactory results have been achieved using a very short polish cycle (2 sec) followed by immediate specimen wash in distilled water
- acceptable images highlighting *joint microstructure* can be obtained using an optical microscope, whereas *cracks* in the solder joints are usually better located using an SEM in the secondary electron mode
- the SEM technique does require a conductive coating (e.g. AuPd, Au or carbon) over the specimen. The level of polishing should be minimised by examining the specimens in the SEM back scattered electron mode, which is well suited for qualitative and/or quantitative analyses
- a technique called “digimap” (i.e. mapping selected elements in distinguishable colours) can also be helpful when used in applications for coatings and laminate.

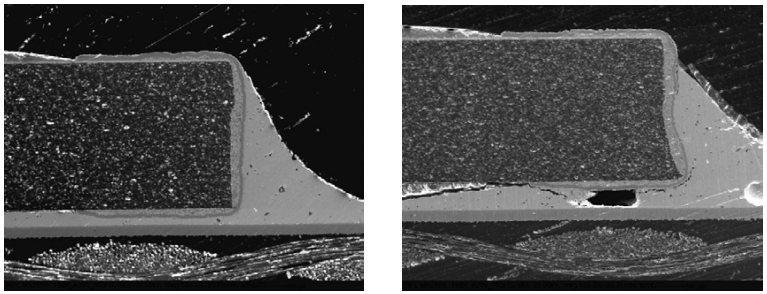

Figure 2. Microsections of 2512-type resistor solder joints without a crack (300 cycles - left) and cracked (after 900 cycles - right). The images were taken in the SEM secondary electron mode

Although the micro-sectioning technique is valuable for the assessment of the failure mode, it can be misleading for quantitative evaluation of crack growth in the solder joints. For example, if the plane of sectioning coincides with the mid plane between the ends of the component, the cracked area may not be visible in the microsection [1]. Hence to ensure crack detection the cross-sectional plane should be close to the soldered ends of the component, but this may be difficult with small component sizes, such as 0805-type (or smaller) resistors.

The micro-sectioning technique is the most suitable method to identify and locate cracks and to study changes in microstructure after thermal cycling. Although the method can encounter problems when identifying cracks in small component solder joints, this disadvantage can be offset by investigating the microsections in an SEM rather than in an optical microscope. The method is suitable for qualitative analysis of solder joints throughout their life-time.

4. Dye Penetration

Dye penetration is another traditional destructive technique used for locating cracks, and for evaluation of their nature and extent. A suitable evaluation procedure might include the following:

- The assemblies should be cleaned in an ultrasonic bath in a solution of 50% water, 50% iso-propyl alcohol, and dried using compressed air
- The assemblies should be inserted into a vacuum bell and immersed in Rocol Layout Ink Fluid (red or blue) dye, with a partial vacuum applied for 15 min
- The dye should be cured on the assemblies by baking in a convection oven at 50°C for 10 minutes
- The components should then be removed by twisting with pliers
- Acceptable images of any dye penetration in the joint can be obtained using an optical microscope. A typical image is presented in Figure 3, in which the white line highlights the cracked area
- The crack area growth in terms of the number of cycles can be obtained by measuring the number of pixels in the appropriate part of the image

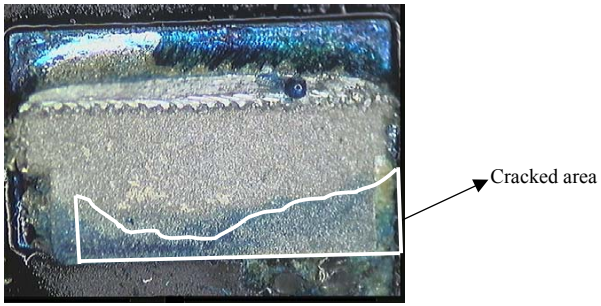

Figure 3. Crack in a SnAgCu solder joint after thermal cycling

This method is capable of providing more quantitative results than can micro-sectioning. It can be used for the assessment of non-cracked areas i.e. to study the stress acting on a solder joint, and to analyze the whole area of a crack. It is not dependent on the positioning of the cross-sectional plane. as is the case with micro-sectioning.

5. Mechanical Tests

Data from mechanical testing provide information on the materials properties of the solder (i.e. deformation) when the joint is subjected to an external load. Such deformation is measured as displacement as a function of time or the number of thermal cycles.

5.1. Shear Test

Shear testing is an established destructive method for evaluating not only the degree of crack propagation and damage to the solder joint, but also the general strength of the joint [2]. The method is based on the assumption that the presence of a crack in the solder joint, its size and the extent of its propagation, will influence the strength of a joint. Hence a correlation can be established between the strength of the solder joint and joint failures.
Figure 4 shows a typical shear test set-up on a Dage Series-4000 modular multi-function bond-tester.
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The following steps are useful to assist good shear testing:

- The substrate should be cut into sections suitable for the holding jig, using a water-cooled diamond saw, which produces a clean edge with minimum stress to the board
- The sections should be cleaned using iso-propyl alcohol to remove any contaminant residues from the cutting stage, and then dried using compressed air
- The stand-off height should be set at h/2 (typically 80 µm) between the bottom of the shear tool and board surface (h is the stand-off height between the component and the board surface). This is the most important test condition
- During each test, the shear tool should be moved forward at an appropriate speed (200 µm/s) against the test component, and the applied force increased until the attachment breaks
- Test data are conveniently analysed [2] in terms of the ultimate shear force (USF) required to rupture the solder joint, and plotted as a function of the number of thermal cycles to which the assembly had been subjected.