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The cover design depicts the microwave planar near-field scanner being developed at NPL.

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A many-cycle phase detector applied to an interferometer for velocity control.

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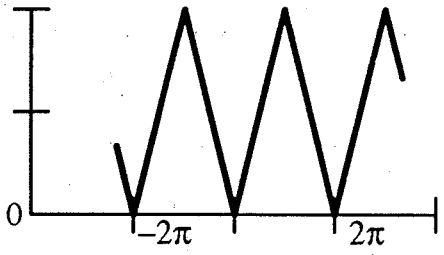
Introduction

The phase detector compares a frequency proportional to the velocity of an object to a reference frequency. Its output is a voltage proportional to the phase difference between the two frequencies over a range of a multiple of 2π radians. This dynamic range, which is greater than that of conventional detectors, simplifies the construction of a servo-system to maintain the average velocity of the object despite disturbances caused by ground vibration and by changes in the demanded velocity.

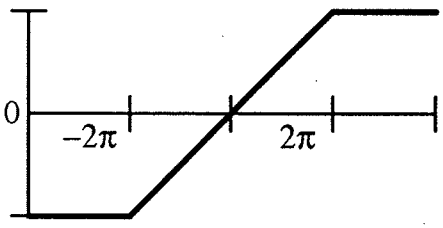
Phase Detectors

Conventional phase detectors can be classified into periodic and aperiodic types. The exclusive-or gate is an example of a periodic detector; it provides an average output voltage which is periodic with the phase difference between its square-wave input signals and is linear over a range of 0 to π radians (Fig 1a). However, if there is a significant difference between its input frequencies its output is a voltage containing sum and difference frequencies and this complicates the process of obtaining a rapid and reliable phase lock. The phase-frequency detector is an example of an aperiodic detector which is used in commercial integrated circuits [1,2]. It has a linear range of $\pm 2\pi$ radians (Fig 1b) and moreover, if there is a significant difference between the input frequencies, its output is a constant voltage which indicates the sign of the difference. This simplifies the locking process.

The detector described below is aperiodic with an increased linear range. Furthermore, it can accept two-phase input signals so that the sign of the velocity can be sensed from the phase relationship between phase-quadrature signals.



(a) Periodic



(b) Aperiodic

Figure 1

Description of Apparatus

This novel phase-detector has been applied to the moving-coil apparatus. [3]. The velocity of a coil suspended from the arm of a balance is measured using a laser interferometer. The interferometer produces two output beams whose interference patterns are in phase-quadrature. Two photodiodes detect the resulting optical signals; the electrical signals are then amplified and converted to TTL levels.

Figure 2 shows a simplified circuit diagram of the phase detector which, with the exception of the Digital To Analogue Converter (DAC), is contained within a single programmable-logic integrated circuit. The in-phase signal from the interferometer is applied to the input of two series-connected D-type flip-flops whose outputs are combined by an *and* gate. This circuit detects positive edges at its input and its output is synchronised to a clock signal ϕ which is chosen to be some tens of times higher than the highest expected input frequency. The output of the *and* gate goes *true* for one clock cycle following a *false* to *true* transition on the input. The output is sampled at the mid-point of a clock period to allow time for any meta-stable states to decay. A further *and* gate combines the edge detector signal and the quadrature signal to produce a signal which determines the direction of count. The quadrature signal is not passed through a synchroniser as its level does not change during a transition on the in-phase channel. An identical circuit is used to process the reference signal except that the quadrature input is replaced by the 'Move Up' signal which determines the eventual direction of controlled movement.

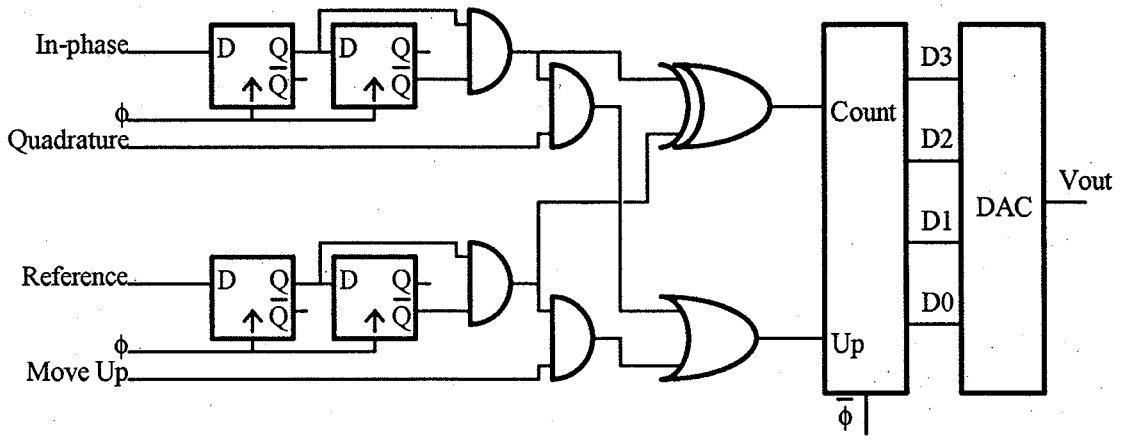


Figure 2 Circuit diagram of phase detector.

The counter consists of four flip-flops and logic to prevent it counting up past full scale or down through zero. It has two inputs: Up determines the direction of count, and Count, if *true*, allows a count operation to proceed on the next rising edge of the counter clock signal $\overline{\phi}$. When the phase difference is near zero the count up and count down pulses may appear simultaneously; the *exclusive-or* gate preceding the count input then ensures that no count occurs. The output of the counter, which can be represented as a number in the range 0 to 15, is connected to the four most significant bits of the DAC. Each count produces a change V_d in output voltage with zero volts corresponding to a count of 8. Each whole count represents a change of phase of one cycle between input and reference. Whenever the phase difference is a not a whole number of cycles and the count up and count down pulses are separated by at least one clock period the counter will increment and then decrement. This makes the DAC output switch between adjacent levels with a mark-to-period ratio equal to the fractional part of the phase difference between the inputs. The resolution is the clock period divided by the reference period. The relationship between the average output voltage V_{out} and the phase difference $(\phi_r - \phi_i)$ (in radians) between the inputs is $V_{out} = \frac{V_d}{2\pi}(\phi_r - \phi_i)$ in the range $-8V_d < V_{out} < 7V_d$. The resolution is limited by the clock frequency at high reference frequencies or by non-linearities in the DAC mark to space ratio otherwise.

The DAC output voltage is converted to a current which is passed through a coil attached to the balance arm. The coil is placed in the field of a permanent magnet so as to exert a force on the balance arm. This force acts to equalise the frequencies of interferometer and reference. The servo so formed is damped by combining the DAC voltage with a voltage proportional to its first derivative.

Figure 3 shows the operation of the servo to slow down and reverse the motion of the balance arm. Initially the balance arm is moving up and the quadrature signal is *false* whenever a positive edge occurs on the in-phase input, thus causing the counter to count down. Since the 'Move Up' signal has been set *true*, positive edges on the reference input cause the counter to count up. These opposing effects hold the servo in equilibrium with a small phase difference between the inputs producing a small average voltage from the DAC which provides the force to move the balance arm. When the 'Move Up' signal is set *false* both in-phase and reference edges cause the counter to count down, eventually reaching a limit of 0. This will cause the balance arm to slow and eventually start moving down, whereupon the quadrature signal becomes *true* whenever a positive edge occurs on the in-phase input causing the counter to count up. As the balance arm gathers speed the counter will then cycle between 0 and 1 as it receives reference edges and in-phase edges. Once the in-phase frequency exceeds the reference frequency the counter will count up past the equilibrium point. Eventually equilibrium will be restored with the balance arm moving down with its speed controlled.

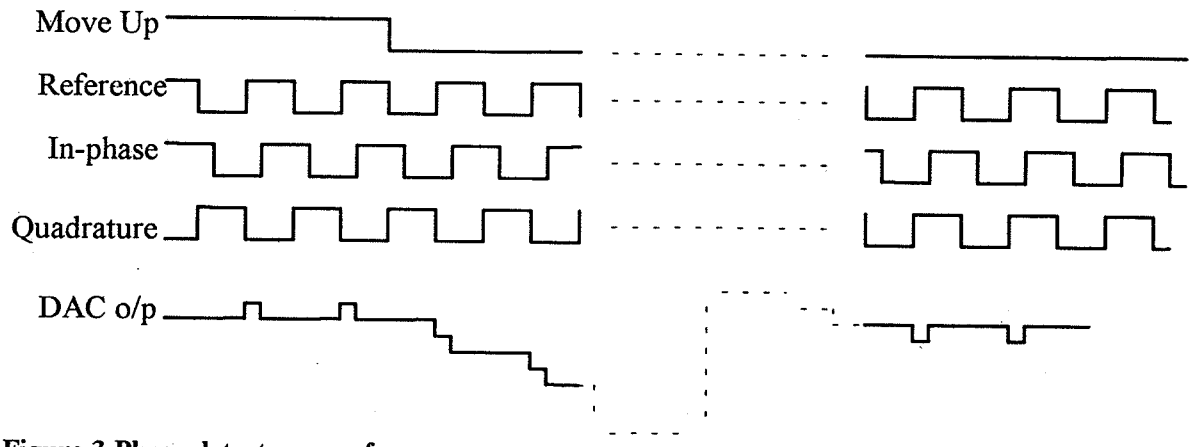


Figure 3 Phase detector waveforms.

Performance

The control system maintains the average velocity of the balance arm constant to within 1 part in 10^5 over a period of 1 second. At present a 20Hz mechanical resonance within the apparatus limits the performance of the servo.

Conclusions

This phase detector is useful in servo-systems which maintain long-term equality of two frequencies in the presence of large short-term disturbances. In addition it simplifies the adjustment of the natural frequency and damping coefficient of such a system using an oscilloscope connected to the DAC output. A step-function is induced in the reference frequency which produces a damped sinusoidal phase-difference extending over several cycles. This waveform is monitored by the oscilloscope showing the effects of any adjustment. Conventional phase detectors would clip the waveform and make interpretation difficult.

References

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