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Test Methods for Evaluating the Reliability of PCB Finishes using Lead-Free Alloys - A Guide

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ABSTRACT

This guide recommends and details best practice for short-term accelerated thermal cycling as a method of assessing the compatibility (and hence joint reliability) of lead-free solders with the materials of the PCB assembly. The assessment involves electrical continuity and shear test measurements complemented with microstructural observations. Data for various PCB materials assessed using the test method described are reported in MATC(A)89 'Compatibility of Lead-free Solders with PCB Materials'.

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1. INTRODUCTION

Electronics assemblies are manufactured from a range of materials with different coefficients of thermal expansion (CTE) – see Figure 1 for a cross-section of a typical joint. As these assemblies experience temperature/power changes during use (e.g. power consumption; switching equipment on/off; day/night temperature changes) the CTE mismatches place shear strains on the various components in the assembly. It is a function of the materials used in assemblies that these strains are relieved in the solder joint, which becomes damaged as a consequence of continual thermal excursions. Such strains can result in crack initiation (usually in the solder joint under the component), subsequent crack propagation through the solder fillet, and finally failure of the joint. Thermal cycling, which accelerates the development of the cracks and structural changes that weaken the solder joint, can therefore be conveniently employed in accelerated testing of the joint, geared at assessing their reliability.

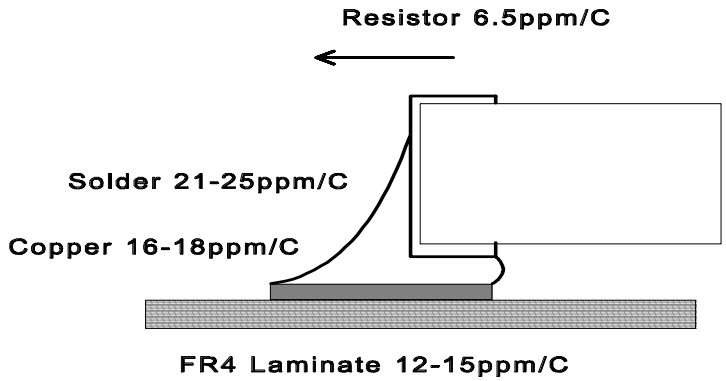

Figure 1: Schematic cross-section of a SM assembly highlighting the CTE (X-axis) mismatches.

A traditional method for assessing reliability has been to use electrical continuity measurements, which provide a technique in which a large number of joints can be monitored. However, the technique is dependent on a complete electrical failure occurring before any defect is registered, which can be a sever disadvantage when 200-5000 cycles may be required to reach a failure. Consequently, another complementary technique is often also used – i.e. the measurement of the solder joint strength, which will be a complex function of microstructural damage, and specifically the degree of crack propagation. A method based on shear testing for the evaluation of accelerated thermal cycling is one that has been used recently for reliability assessment and lifetime prediction (1).

In this Best Practice Guide the use of both electrical continuity testing and shear strength measurements are recommended, supported with complementary observations from solder joint microsections. It follows the procedures discussed in a sister report (2). The detailed results of an investigation of the compatibility/reliability of lead-free solders and pcb finished undertaken using this Best Practice, has been recorded elsewhere (3).

In Figure 2 there is the flow diagram of reliability assessment described in the Best Practice.

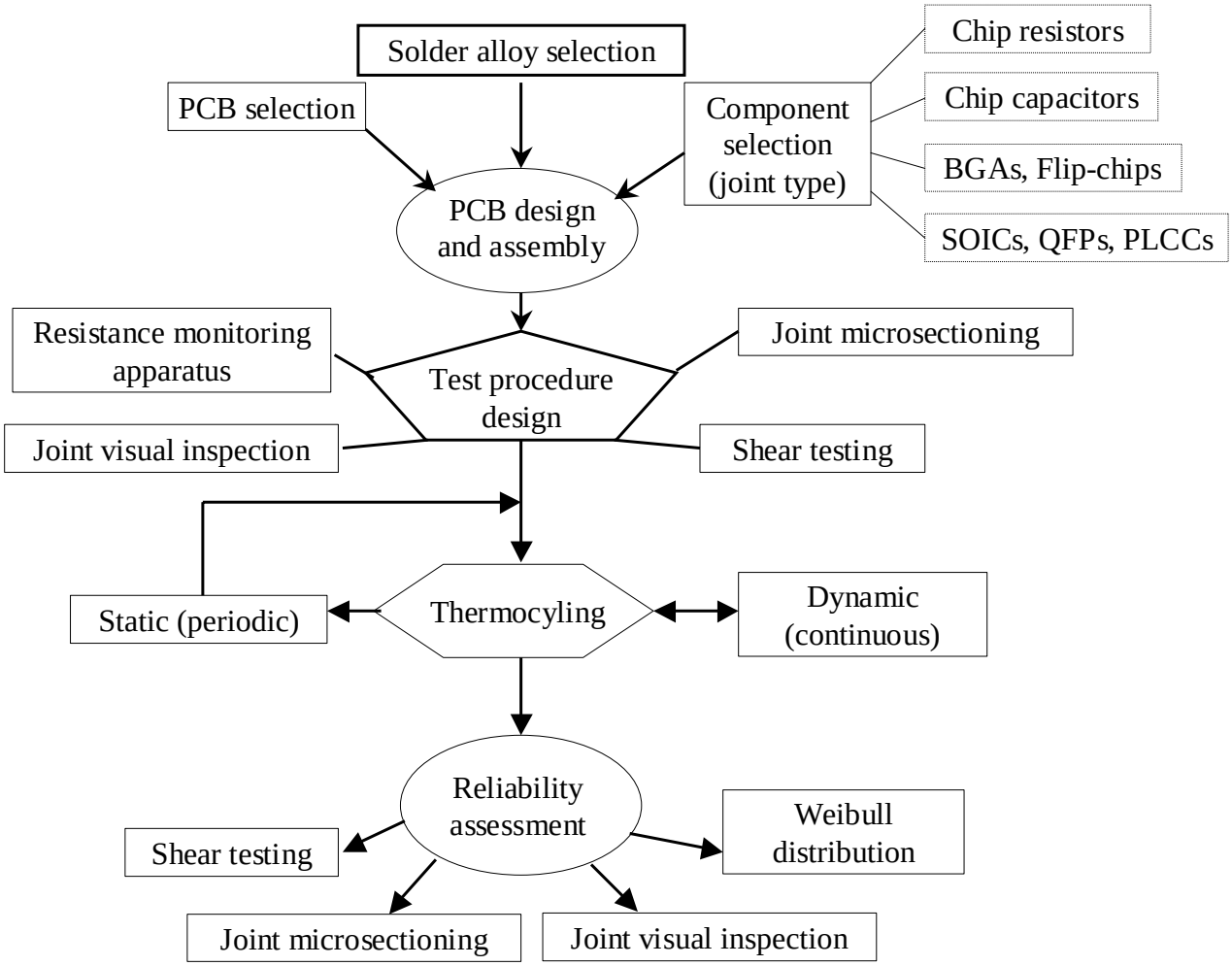

Figure 2: Flow diagram of solder joint reliability assessment

2. TEST ASSEMBLIES

2.1. General Approach

A critical consideration in any reliability assessment of solder joints is designing the test vehicle, the approach to which must be to eliminate as many variables as possible, thus achieving a closely focused test. The main features of the test will then be the solder material, joint geometry, component solderability, or any other particular experimental parameters that needs to be investigated. The design of the test vehicle mainly centres on the materials used for the base substrate, components and solder.

The selection of materials may restrict the number of component types that can be used, since component termination finishes are available in only a limited variety. It should be noted that the selection of solder and base materials will mainly affect long-term reliability, whereas the selection of component types can be more significant and influence short-term reliability.

2.2. Component Selection

The physical aspects of components can have a very significant effect on reliability and so dominate the experimental response when assessing solder joint reliability. This can be used to advantage to obtain joint failures over a wide range of thermal cycles. Indeed, in order to enhance failure rates, known “weak links” should be selected for the testing. These “weak links” are components in which the CTE mismatch is high, and in which early joint failure might be expected, and for which failures have been reported in commercial product. Typically this involves the use of components such as ceramic resistors/capacitors (where the mismatch increases with size from 0603-type to 2512-type), BGAs, flip-chips, through-hole connectors etc. Gull-wing or “J” leaded parts are usually far more robust due to the compliant nature of the lead.

The component terminations should ideally not contain lead, since its presence complicates the analysis of the failure data for a supposedly fully lead-free system. Small additions of lead do significantly alter processing, for example, wetting is enhanced over that of a lead-free solder alloy.

Some components found to be suitable for use in compatibility/reliability testing are:

Chip resistors. These are often used because their rigid alumina bodies have a significantly different CTE from the other materials (see Figure 1) and hence are more prone to fail from stress accumulation in the solder joints. The magnitude of the effect is dependent on the component size. Typically the largest available is the 2512-type and it is prudent to complement this choice with a more frequently used component size, such as the 0603-type. Another advantage of using chip resistors is the simplicity of joint failure detection i.e. a high resistance or an open circuit is easily detected by a simple DC measurement. Currently there are two commercially available termination finishes for these components, Sn and SnPb.

Chip capacitors. These components require a more sophisticated detection method (AC response or pulse-response detection). There are two main capacitor types: multilayer (bipolar) chip capacitors and tantalum (unipolar) electrolytic capacitors. Both are sensitive to high temperatures and their (component) reliability can be lower than their solder attachment.

SOIC, QFP, PLCC. The attachment design is based on the gull wing or J-lead types, arguably the most common types of lead attachment used in SM assemblies. The heel of a solder joint provides a good indicator of wetting acceptability and hence can be used to focus visual inspection. Since this type of attachment is compliant, its reliability is considered to be high providing that proper wetting characteristics have been achieved (4). Use of these components should be limited to daisy-chained patterns that facilitate ready DC continuity failure detection, and SOIC packages such as resistor networks are an ideal choice of components. Gull-wing SOICs are available with a wide range of termination finishes.

BGA, Flip-chip. The use of bump or ball type of attachment is a space-saving option especially for high density packages. The solder bumps can comprise the same (or different) materials as the solder. There are some high melting point solders used on some BGA designs. Again a daisy-chained pattern between the solder balls is desirable. It is essential that the component has a silicon die inside the package, since the die significantly influences the stresses within the package, which will in turn have an impact on the solder joint performance

There are some requirements regarding the number of component parts to be used in the test, and it is vital to test a sufficient number to ensure the results are statistically significant. The planned number of experimental variables together with factors such as the chamber size, will also influence the final experimental plan. From purely statistical considerations the optimum number of uniform samples for any test is 110, based on the binomial distribution and assuming 95% confidence interval. A 5% uncertainty interval is achieved when only one failure occurs in 110 uniform samples (4).

2.3. Board Selection

The choice of board finishes to be tested should reflect not only those for potential use in particular lead-free soldering technologies relevant to the product and/or industry of interest, but also those in current widespread use (for bench-marking purposes). Other factors to be considered are the availability of boards with specific finishes, the component termination finishes, and the assembly method(s) of relevance. Typical board finishes are :

Cu/OSP; immersion tin; immersion silver; AuNi; HASL, SnPb

Wherever possible the board finish should be applied using commercial processing systems.

2.4. Board Design

The design of the board is a key element in achieving successful testing. Not only should the substrate material be representative of the assemblies being evaluated, but the design of the pads and tracking will also need to meet the functional requirements of the components to be

tested. In particular, for the electrical continuity measurements, this requires the boards to match the daisy-chained aspects of the parts to be tested. Other issues to be considered include how the parts will be cut from the pcb for later microsectioning and shear strength testing.

An example of a suitable pcb layout is shown in Figure 3. It is fabricated from a double-sided FR4 substrate with photo-imagable resist, dimensions 122 x 113 x 1.6 mm, and copper tracks 35mm thick. The design incorporates 20 off 0603-type resistors, 20 off 2512-type resistors, 40 off TH resistors, 2 off BGAs, 2 off CSP, 10 off SOICs, 20 off DIPs, 1 off PGA, and one 3 x 32 pin connector. All the components, except the edge connector, are connected to the edge connector to facilitate the electrical continuity measurements. This pcb and other designs are available from: www.npl.co.uk/npl/ei.

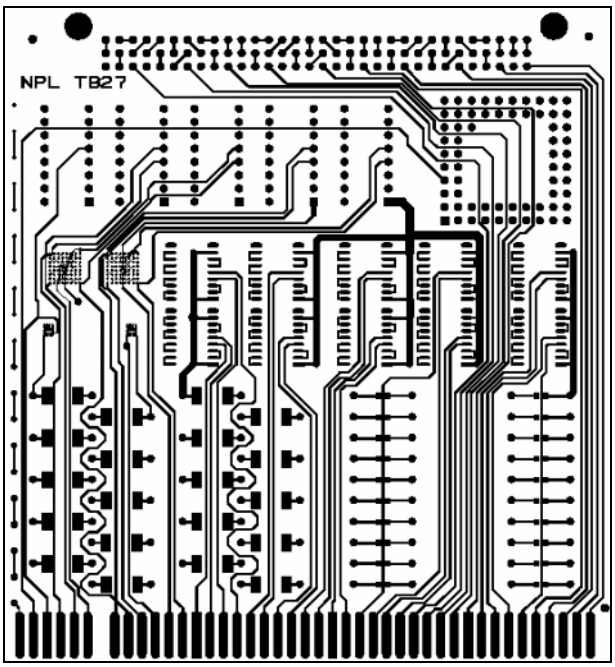

Figure 3: Example of a suitable test board layout

2.5. Board Assembly

The process chosen to assemble the test vehicles should be representative of those used for assembling the product(s) of specific interest. Care should be exercised to ensure that all the test vehicles are assembled under identical conditions, and ideally in one batch to avoid introducing further assembly variables that may influence the test results. Stencil printing, component placement, and other factors can be key in influencing any assessment outcome. For example, the height of any solder joint has a significant effect on reliability, and hence printing and component placement need to be consistent and carefully controlled.

The number of test boards assembled will clearly depend on the number of parts on each board and the number of experimental variables. Consideration should also be given to the number of samples that will be required for subsequent microsectioning and shear testing.

Since these tests require pcbs to be removed during the test procedure, it is essential to ensure sufficient pcbs remain for the electrical continuity measurements.

Codes of Practice for solder paste, stencil printing materials, and stencil printing have been previously reported (3) and should be followed whenever possible. Here it is recommended that a stainless steel stencil be used having a thickness of 100 mm over the general components area, and 200 um over the connectors area, the additional thickness being achieved using a nickel foil. A suitable stencil design for the chosen board design is presented in Figure 4. It incorporates three alignment fiducial marks to facilitate precision alignment. The solder paste should ideally be printed with an automatic printing machine under constant temperature and humidity conditions (e.g. 22°C and 40%RH). A controlled temperature/humidity is desirable, though not essential.

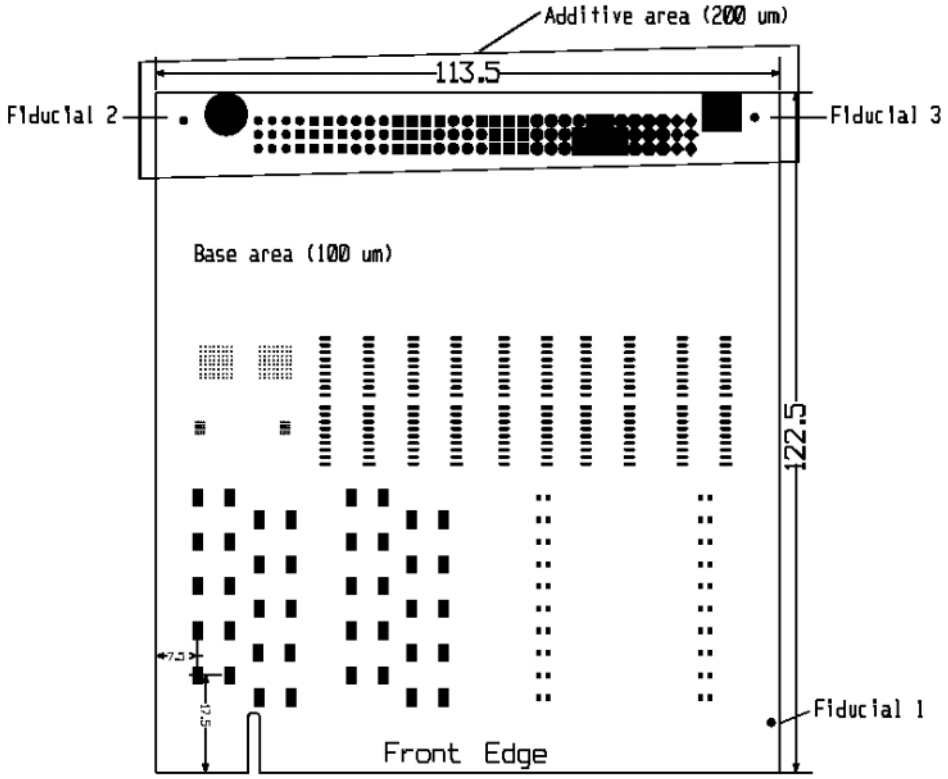

Figure 4: Example of a stencil design for the test board

Any components prone to the phenomenon of “pop-corning” or blistering from entrapped moisture during soldering, and this certainly includes many BGA and CSP components, should be pre-baked according to the component manufacturers’ recommendations. A typical pre-bake is one hour at 125°C. Whenever possible components should be placed using an automatic pick and place machine. Surface mount components that are to be wave-soldered should be attached to the boards using a commercial surface mount adhesive (SMA) dispensed automatically. A typical SMA curing regime is 90 minutes at 150°C. Suitable convection reflow soldering temperature profiles (3) for both lead-containing and lead-free solders, are shown in Figures 5 and 6 respectively.

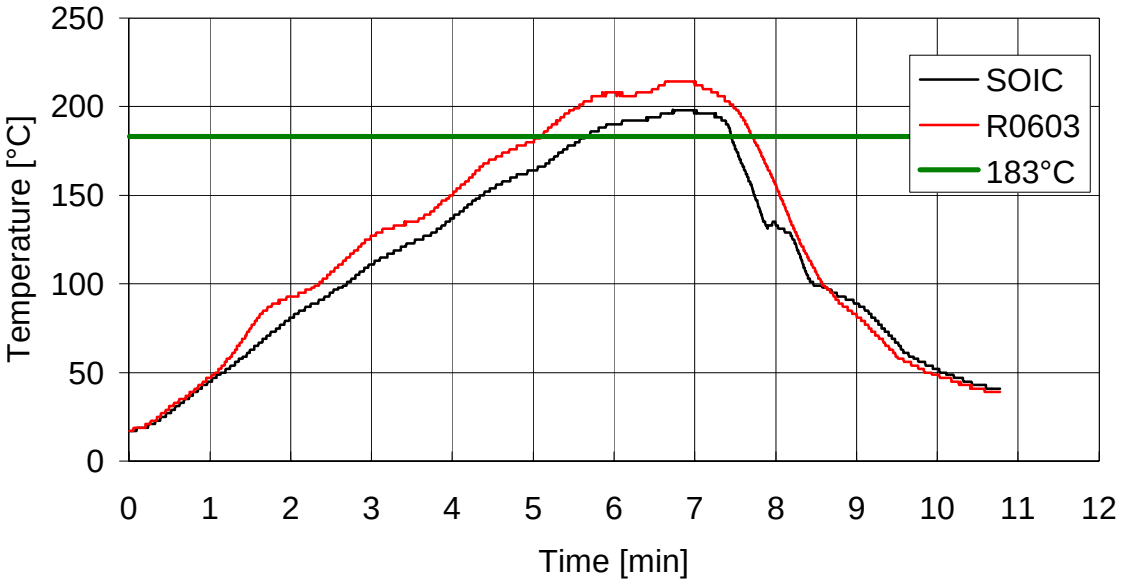

Figure 5: Typical reflow temperature profile for SnPb solder

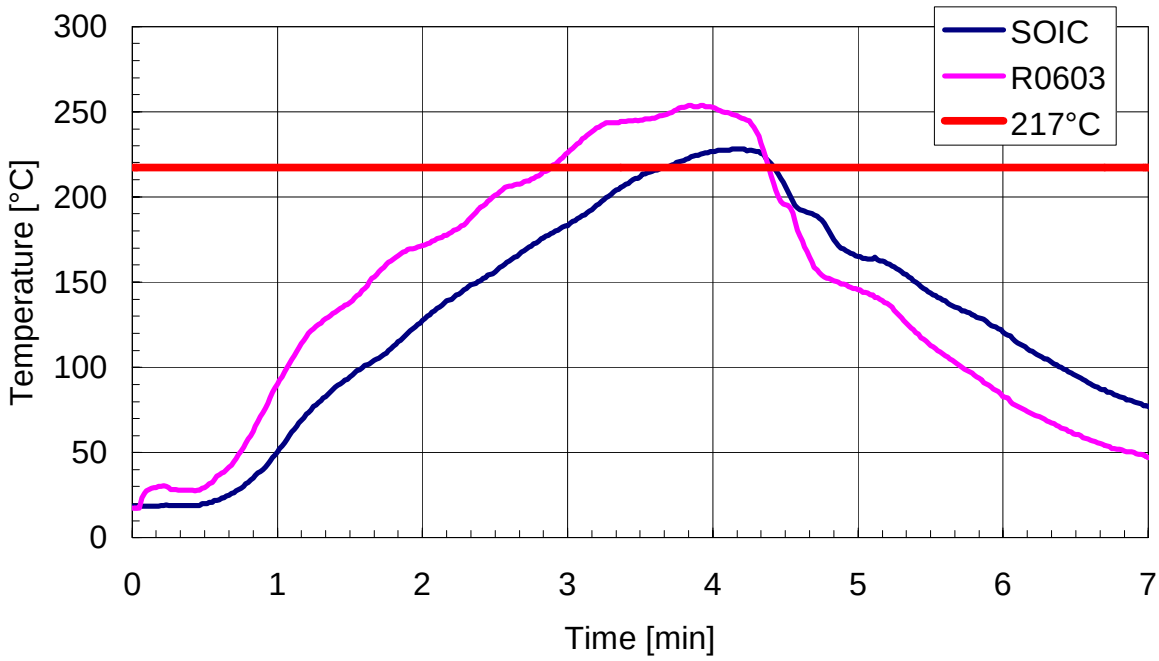

Figure 6: Typical reflow temperature profile for lead-free solders

For wave-soldering trials it is recommended that a conveyor speed of 1.2 m/min is suitable, with a soldering temperature of 250°C i.e. approximately 35 degrees superheat depending on the lead-free solder under test. Since, for the purposes of these compatibility tests it is desirable to ensure good wetting of all the joints, it may be necessary to spray the board and solder wave with a suitable flux (e.g. rosin-free, RF 800T).

2.6. Thermal Cycling

The choice of the cycling regime used to evaluate the compatibility/reliability of the solder joints is crucial. The following factors, the greater the temperature range, the shorter the cycle, and the larger the number of the cycles, all increase the stress on the solder joints. But it is vital that the regime selected should reflect the likely working environment of the product(s) of interest (e.g. military, automotive, consumer etc). In recent years the military and automotive sectors have preferred to use the same cycling regime, and this now appears suitable for many, if not all, applications (5). The temperature profile of this regime is illustrated in Figure 7. The test cycles between –55°C and +125°C with five minutes dwells, the latter being defined as the time during which the temperature of the cycling oven was within ±5°C of the set value.

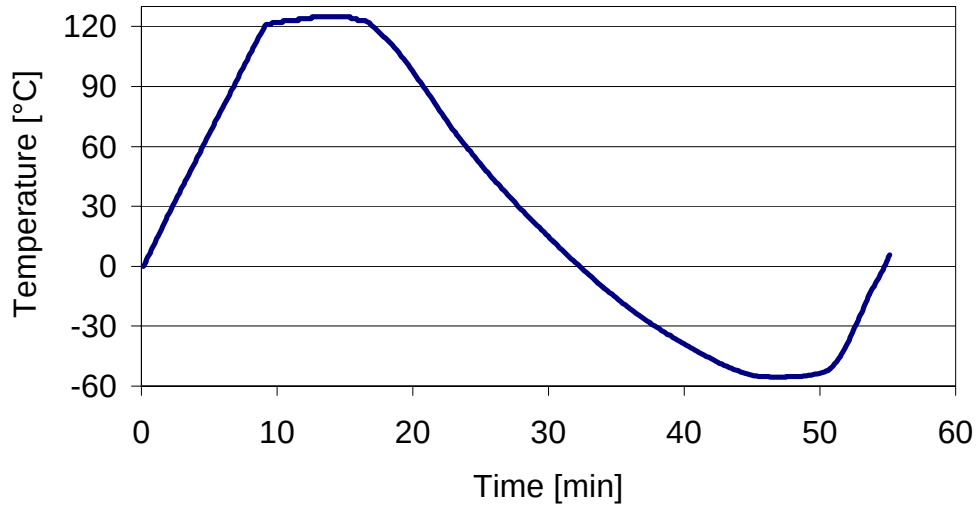

Figure 7: Typical temperature cycling regime

Since it is desirable to have a uniform temperature distribution in the cycling chamber, it is recommended that forced airflow circulation be used to achieve this. In addition, in order to minimise any impact both of temperature variations within the chamber, and of different heating/cooling rates, the position of the sample boards should be regularly varied inside the chamber.

3. DATA ACQUISITION

3.1. Electrical Continuity Testing

Electrical continuity measurement is a well-known and widely used DC method for assessing solder joint reliability. Although it allows large numbers of joints to be monitored, it does rely on a complete open circuit (i.e. fracture) before any failure is registered. A big advantage of the electrical continuity testing is that there is no presumption on when failure occurs, and

no samples are consumed during measurement. Hence testing can easily be carried out for a few hundred or a few thousand cycles. There are two basic methods of carrying out the test:

Static (periodic) monitoring:– multiple boards can be tested sequentially using only one measuring connector, permitting a large number of boards to be assessed. However, there is a low confidence level of detecting the first failure, and hence the recorded number of cycles to failure will be higher, the actual level depending on the measurement frequency.

Dynamic (continuous) monitoring:– has a high probability of capturing a failure. However, the monitoring capacity is restricted by the number of monitoring channels, and hence the number of boards in the test. Another issue lies with the integrity of the board connections inside the chamber under exposure to the thermal cycling.

Unless fast transitions in resistance levels, such as in telecommunications applications, are required, the static monitoring approach is recommended as the preferred test routine, with measurements taken at room temperature typically after periods of 100-200 cycles. All the components connected in the circuits for continuity measurements should be tested in the as-assembled condition (i.e. prior to thermal cycling). They should all exhibit an electrical resistance within the manufacturers' tolerance of ±5%, and all resistance data should be recorded and filed for future use. After each set of cycles the resistances are again measured, and if any channel resistance increases by >10% above its nominal value a "failure" is recorded. In practice mechanical failure of the joints results in resistance changes of several, orders of magnitude in very short timescales.

A schematic of a suitable measurement circuit is presented in Figure 8 and has the following features

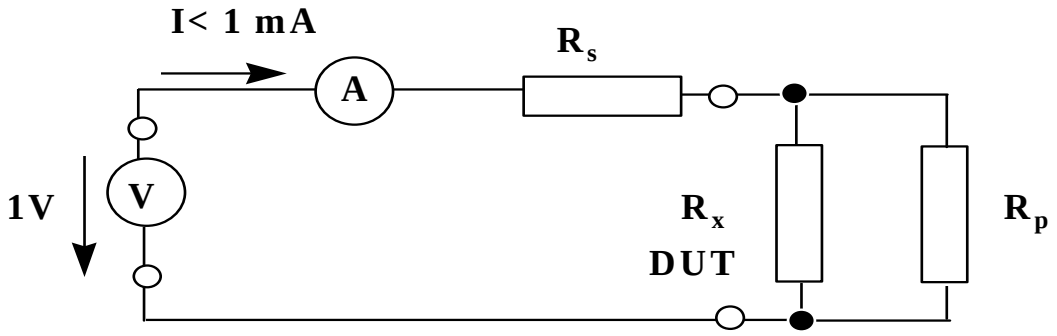

Figure 8: Schematic circuit for the measurement of electrical continuity

- Each board is connected via an 80-way switch bridge to a multimeter
- A resistor Rs is used to limit the current to <1mA to avoid any partial melting of the fracture/crack surfaces
- A resistor Rp (1MΩ) is connected in parallel across the device under test (DUT)
- A schematic of a suitable electrical continual testing set-up is shown in Figure 9, and has the following features
- Measurements are computer-controlled using LabVIEW® software
- A computing multimeter SI 7151 is used for either temperature monitoring on the board whilst thermal cycling OR for electrical continuity measurements
- A switch system Keithley 7011 is used to select the proper measurement channel

- The SI 7151 and 7011 instruments are connected to a computer and controlled by LabVIEW® applications
- Resistance data are stored as an ASCII file for later analysis

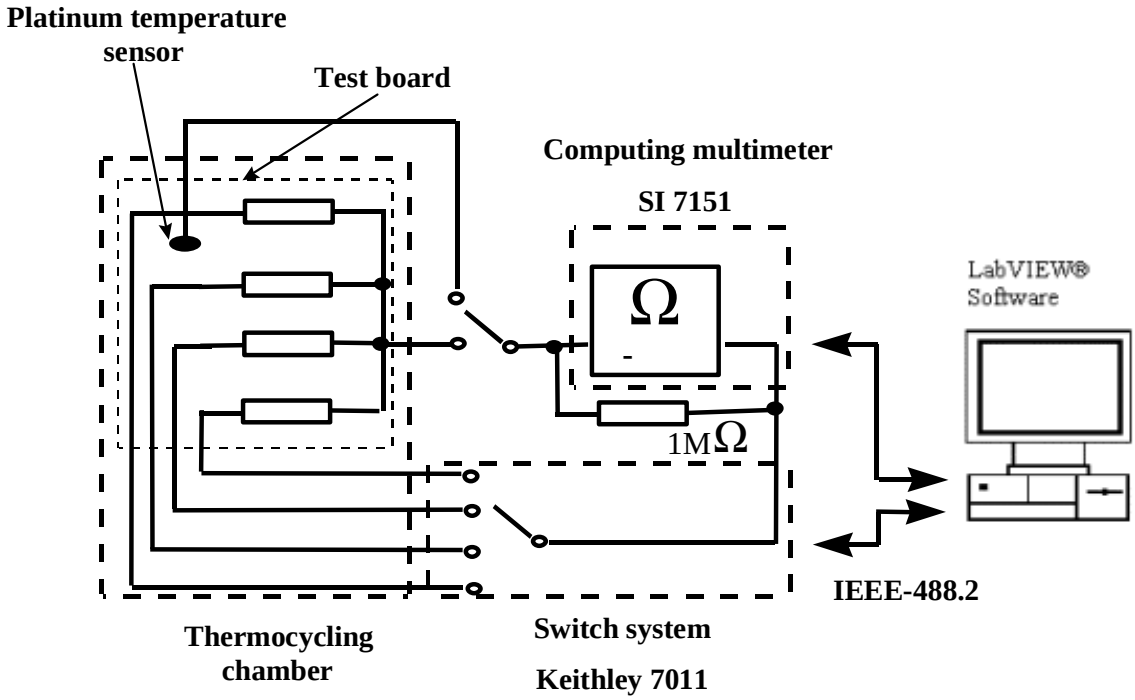

Figure 9: Schematic of electrical continuity test equipment

To maximise the usefulness of the data, it is appropriate to fit a Weibull distribution to the cumulated failure data in order to obtain the failure rate, and the $N_{f,50\%}$ median number of cycles (for 50% cumulative failures), $N_{f,62.3\%}$ the characteristic number of cycles (62.3% cumulated failures) and the slope factor β (see reference 6). The errors of these resistance measurements depend on the probability of a failure detection (7) and the sampling rate of continuity measurements (8). The analysis of resistance data from a previous exercise demonstrates the value of this analytical approach for evaluating lead-free solder compatibility (3). Indeed, an analysis of the slope factor as a function of the characteristic number of cycles to failure, allowed clear differentiation between the performances of lead-free and lead-containing solders in terms of compatibility with various board finishes.

3.2. Shear Testing

Shear testing is an established destructive method for evaluating not only the degree of crack propagation and damage to the solder joint, but also the general strength of the joint. The method is based on the assumption that the presence of a crack in the solder joint, its size and the extent of its propagation will influence the strength of a joint. Hence a correlation exists between the strength of the solder joint and the failure rate. A schematic of a suitable shear test is given in Figure 10.

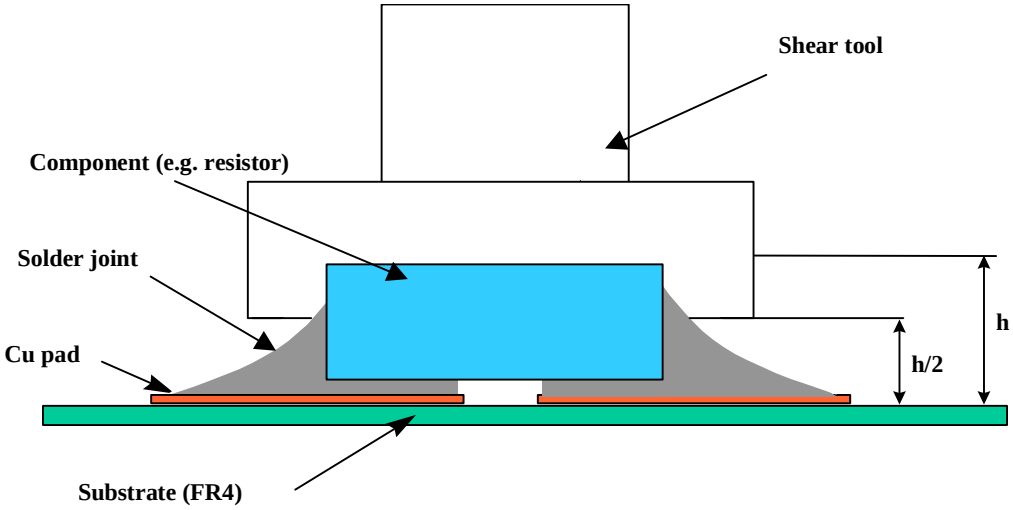

Figure 10: Schematic of shear test arrangement

There are several essential steps in carrying out shear tests:

- The board (substrate) is cut into sections containing 2 or 3 components for testing, using a conventional water-cooled diamond saw, which produces a clean edge with minimum stress to the board
- The sections are cleaned (e.g. with IPA - iso-propyl alcohol) to remove any contaminant residues from the cutting stage, and dried using compressed air
- The board sections, either whole or cut to size, are properly fixed in the shear equipment
- The necessary test conditions are set, of which the most important is the stand-off height equal to h/2 (typically 80 mm), between the edge of the shear tool and board surface
- During each test, the shear tool is moved forward at a defined speed (typically 200 mm/sec) against the test component, and the applied force increased until the attachment is broken.
- The provision of an X-Y table on which to mount the jig whilst not essential, is useful in facilitating ready repositioning of the shear tool directly behind the component

Photographs of a shear test jig and push-off tool before and after a shear test are reproduced in Figure 11. The data obtained in the test can be readily plotted and analysed in terms of the ultimate shear force required to rupture the solder joint as a function of the number of thermal cycles to which it had been subjected (3). A disadvantage of the technique is that since the samples are destroyed during testing, the removal of sample boards should ideally be at the number of cycles of interest, i.e. when failure occurs. Therefore some prior knowledge of the failure range is required. This may not be an issue where assemblies are being built to pass required lifetime criteria at a fixed number of cycles.

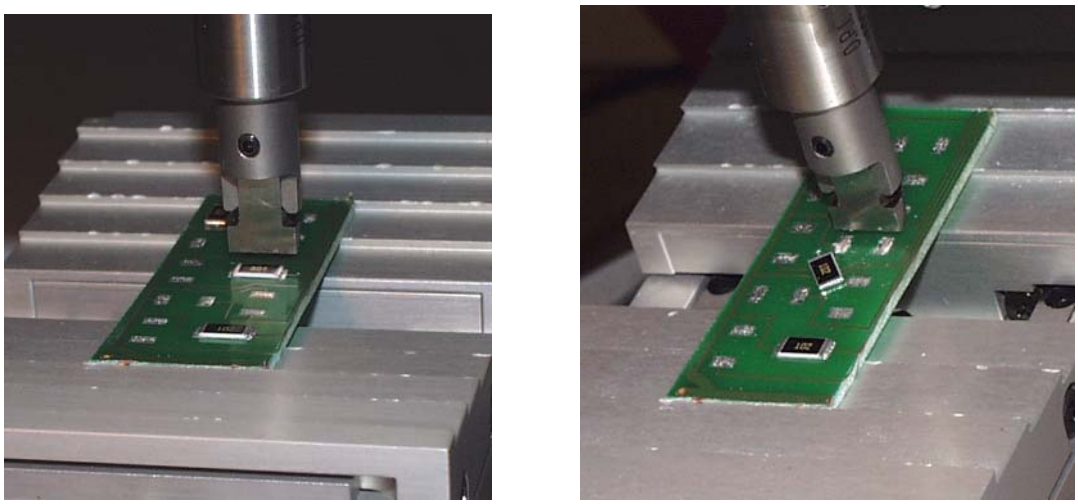

Figure 11: Shear test jig and push-off tool before and after a shear test.

3.3. Microsectioning

Metallographic microsectioning is another widely used destructive method for understanding the behaviour of the solder joints. It is particularly useful for investigating the evolution of the microstructure with thermal cycling and the development of the microcracks. Although no failure data can be obtained, qualitative information on how solder joints fail can be obtained. A suitable procedure is along the following lines:

- Ensure the original experimental plan includes sufficient boards/joints for microsectioning purposes; any of the components used in the test board can be microsectioned
- Cut sample joints individually from the boards using a liquid-cooled conventional diamond saw to ensure that the soldered joints do not experience any significant temperature excursions
- Cut cleaned sample joints using IPA to ensure removal of any cutting residues
- Mount clean samples in cold curing epoxy
- Grind and polish sections using silicon carbide paper (120 to 4000 grit) on automated machines; polish using diamond-containing sprays or pastes with particulates 15-0.25 mm in size. Diamond-impregnation of the cloth should be kept to a maximum to ensure the best cutting rate
- Finally polish by hand using gamma alumina powder suspended in a lapping fluid
- Etch the microstructure: for lead-containing solder systems a solution containing 2ml hydrochloric acid and 98ml industrial methylated spirits is suitable; for lead-free solders better etching is achieved using a solution of 2ml nitric acid, 2ml hydrochloric acid, and 96ml distilled water
- Examine the microsections using standard optical bench microscopes at magnifications up to 200x. A method for recording the images is desirable.

4. INTERPRETING THE DATA

Three methods of collecting data have been described, each providing different, but complementary, data, and it is strongly recommended that a combination of two or three should be used in any assessment of the solder joint/board reliability. Although the electrical resistance continuity data provide a spectrum of failures, monitoring can be time-consuming and expensive. Shear testing is quick, but it is destructive, and hence care must be taken to produce sufficient numbers of boards to accommodate the planned assessment at the predetermined numbers of cycles. Microsectioning is useful in confirming the failure mechanisms and the damage volume induced by cycling. Some level of microstructural investigation to confirm failure modes should always be an integral part of reliability studies.

When characterising a new system it is recommended that electrical continuity measurements should be used, since this test provides detailed data, and makes no assumptions about when failures occur. The generated N_f and β data are also very useful as figures of merit to benchmark assembly performance and yield. On the other hand, when developing an existing assembly, in which small modifications are concerned, shear testing offers a very efficient method of assessment. The results are readily acquired and monitoring is not required throughout the thermal cycle.

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6. ACKNOWLEDGEMENTS

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