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Abstract

The use of cryogenic current comparators at NPL has been limited so far to measurements with direct currents. A new current comparator, designed to work at frequencies of up to 100 Hz, has been built and will form the basis of a bridge for AC resistance and quantum Hall measurements. The relative uncertainty of measurements carried out with the new system will be approximately 10^{-8} .

1. Introduction

While DC measurements of resistors of values below 10 k Ω at NPL in recent years have been carried out using automated cryogenic current comparator (CCC) bridges [1], AC resistance measurements and investigation of the AC quantum Hall effect have been made with coaxial AC resistance bridges based on room temperature inductive voltage dividers. A new system is under development which will extend the range of CCC measurements to alternating currents and which will be suitable for resistance and quantum Hall measurements from DC to 100 Hz. The evaluation of AC/DC properties of resistors at the 10^{-8} level is important for accurate resistance thermometry. The underlying principle for CCC operation is the same at low frequencies as at DC, but it is necessary to compensate for capacitive errors of windings and leads. The new CCC uses a technique incorporating coaxial windings and voltage compensation cores to achieve this compensation. The capacitive errors increase with frequency, so a limit of 100 Hz has been chosen for practical reasons initially, although this may be extended later.

II. Cryogenic Current Comparator for AC Measurements

A. Cryogenic Current Comparators at AC - Capacitive Error

The use of cryogenic current comparators [2] as DC ratio transformers with fractional ratio errors as small as 10^{-10} is well established. At DC, the ratio error of the CCC can be determined by passing equal and opposite currents through equal numbers of turns and measuring the current induced in the detection winding. The detection principle, based on the superconducting properties of the shield, and the associated magnetic error remain the same at AC, as long as the superconductivity is not destroyed and the surface resistance remains negligible. However with AC, shunt and screen capacitances in the windings and the connection leads result in an additional capacitive error.

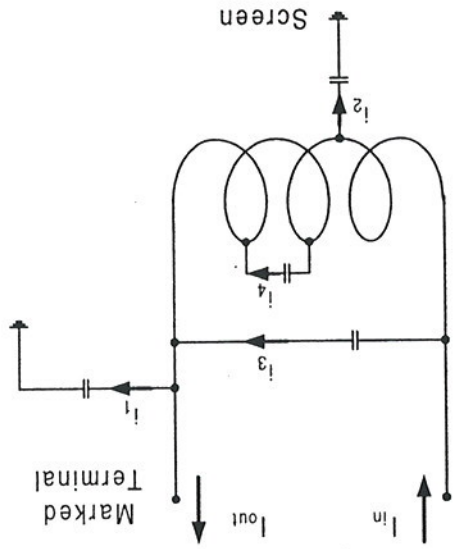


Figure 1: Contributions to capacitive error of winding.

Due to screen capacitances the current leaving the winding will not match the current entering it, $I_{in} \neq I_{out}$. Hence, it is necessary to choose a point of reference, which will be referred to as the marked terminal. Also, currents through the capacitances depend on the potential present on the leads and windings. Therefore, to obtain well-defined errors the marked terminal has to be associated with a reference potential, usually screen potential. The resulting error contributions are shown in figure 1. While the currents i_1 and i_2 through the screen capacitances, which pass partially or fully through the winding but are not present at the marked terminal, cause a positive error contribution, the currents i_3 and i_4 through the shunt capacitances, which skip part or all of the winding but are present at the marked terminal, cause a negative error contribution.

In order to be able to use the described compensation technique it was necessary to choose a CCC design with sufficient space for a coaxial windings with large numbers of turns. For this purpose, a type II CCC (detector winding in the inside, ratio windings on the outside) with 100 mm ID, 120 mm OD and 170 mm height was built. When connected to an RF SQUID, the measured sensitivity per turn of the CCC is $16 \mu A/\phi_0$. Coaxial cable (OD

D. CCC Design

Figure 2: CCC with coaxial winding. The twisted leads are used to sense the voltage across the outer of the winding.

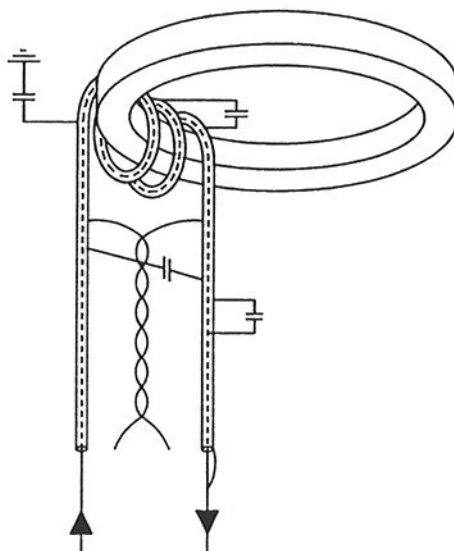
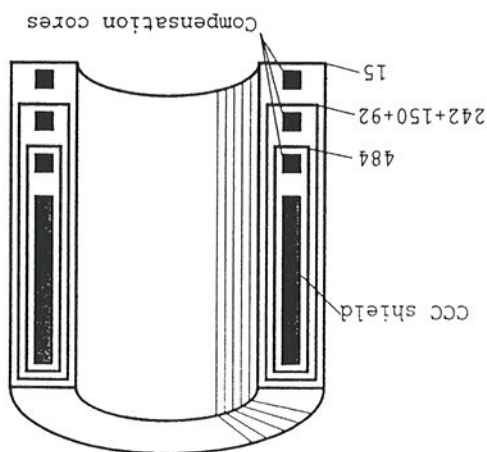


Figure 3: Windings and compensation cores.



The described procedure can only be used if trimming is possible for each independent winding separately. It is not obvious how this can be achieved with a conventional winding. The answer is to use coaxial cable for windings and leads, with the marked terminal outside the cryostat. Inner and outer of the coaxial cable are joined at the marked terminal. As the capacitance of the inner through the outer to the outside can be assumed to be negligible, the inner is free of shunt and screen capacitance. Also, the capacitance between inner and outer does not contribute any error because the outer threads the CCC in the same way as the inner and currents through this capacitance join the main current at the marked terminal where the inner is connected to the outer. Hence, with respect to the inner, the comparator is free of any capacitive error. Unfortunately, this does not hold true for the comparator overall because now the outer of leads and windings have a capacitive error. The relevant capacitances are shown in figure 2. However, it is now possible to calibrate the outer against the inner (which is free of capacitive error) in a 1:1 excitation: the voltage drop across the outer of the winding can be trimmed to zero (the resulting voltage on the inner is irrelevant as it does not contribute any capacitive error). Then, by passing a current through the inner to the marked terminal and back through the outer, and by varying a capacitor between the ends of the outer or the inner and the screen, the capacitive error of the outer can be trimmed to zero. This procedure is carried out for both windings to be used in the measurement and the comparator is subsequently free of capacitive error.

C. CCC with Coaxial Winding

A detailed analysis [3] shows that the error caused by these capacitances can in principle be trimmed to zero for each winding using the following two steps: a high permeability core is placed under the CCC so that the winding passes through the core as well as the CCC with each turn. The voltage across the winding is measured and trimmed to zero by energising the core with an auxiliary winding. In this way the error component caused by the voltage drop along the winding is eliminated. The remaining error can now be trimmed to zero by adding shunt or screen capacitance such that their error contributions cancel each other. The calculation [3] shows that this is possible under the assumption of equal distribution of resistance and inductance along winding and leads.

B. Voltage Compensation and Trimming of Capacitance