

MEASUREMENT OF VERY HIGH LEAKAGE RESISTANCES IN 1 pF CRYOGENIC CAPACITORS USING A SET DETECTOR

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1 pF cryogenic capacitors form an important element of a future measurement system for the small currents generated by single electron pumps [1]. This application sets a stringent requirement on the minimum leakage resistance of the cryogenic capacitor, at $6 \times 10^{19} \Omega$. In this work, a Single Electron Transistor (SET) was used as a sensitive charge detector to evaluate the leakage resistance of two types of cryogenic capacitor. These resistances were found to be $3 \times 10^{16} \Omega$ for fused-quartz dielectric and $> 10^{18} \Omega$ for ^3He - ^4He mixture dielectric capacitors.

Background

Single electron pumps based on small capacitive tunnel junctions offer the possibility of a current standard based on the passage of an exactly known number of electrons through a solid-state device in unit time. Such a standard would be a 'quantum' standard for the Ampere in the same way that the Josephson effect and quantum Hall effects are quantum standards for the Volt and the Ohm respectively. The current from a single electron pump is given by $I = ef$, where f is the frequency at which the pump is operated.

Pump frequencies cannot at present exceed ≈ 10 MHz without loss of accuracy, so the maximum current generated by a pump will be in the region of 1-2 pA [2,3]. For the electron pump to be useful as a metrological device, this current must be measurable to 1 part in 10^8 . The limit of a cryogenic current comparator in resolving 1 pA is approximately 1 in 10^5 , well below the level required. It is therefore envisaged that the current measurement will consist of charging a capacitor with a precisely known number of electrons and measuring the voltage developed across the capacitor plates using a Josephson array voltmeter. If the value of the capacitor was related to the quantum Hall resistance through the conventional impedance measurement chain, the experiment would represent 'closure of the metrological triangle', providing a measure of the ratio $R_K/(h/e^2)$ [1].

To calculate the required minimum capacitor leakage resistance, we envisage that the single electron pump will be run at 6.25 MHz for 1 s, generating a current of 1 pA and charging a 1 pF capacitor up to 1 V. The capacitor must not lose any electrons during the time taken to measure the voltage, which will be about 5 s. To meet this requirement the leakage resistance across the capacitor plates must be greater than $6 \times 10^{19} \Omega$.

Apparatus design

The capacitors were designed to fit into the 25 mm diameter sample holder of an Oxford Instruments top-loading (sample into liquid) dilution refrigerator. Two types of capacitor were under consideration; a fused silica dielectric type with evaporated metal electrodes (fig. 1), and a helium-mixture dielectric type (fig. 2). The dielectric in the latter capacitor was the ^3He - ^4He mixture of the dilution refrigerator, and the plates were separated from the outer shield by 1.5 mm diameter sapphire balls.

To measure the leakage resistance, the voltage source was programmed to apply a step voltage to the cryogenic capacitor, and then return the voltage to its original value after a few minutes. During this time, any leakage through the capacitor would change the voltage on the SFT gate capacitor, and result in a modulation of the current through the SFT. For some experiments, the SFT current was measured by superimposing a small ac modulation onto the source voltage, and

A circuit diagram of the cold part of the apparatus is shown in fig. 3. The SFT bias voltage was set at its optimal value, which for a typical SFT device was close to 1 mV. At the optimal value of bias voltage, the largest modulation of output current is seen as a function of gate voltage [4]. This is the basis of using the SFT as a sensitive voltage detector. The value of the gate capacitance C_G was measured by removing the capacitor C (so that $V_G = V$ in fig. 3), and observing the oscillations in output current as a function of V_G . The period of the oscillations in V_G is equal to e/C_G . C_G was typically between 30 and 80 aF, depending on the SFT device used. With the cryogenic capacitor connected in series with the gate capacitor, the cryogenic capacitor and its stray capacitance to ground act as a voltage divider, and the value of the stray capacitance can be deduced from the apparent periodicity of the SFT oscillations in the source voltage.

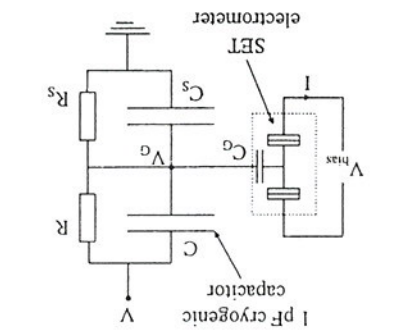
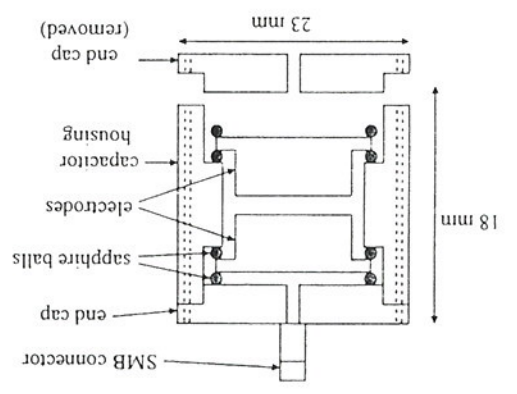


Figure 3 Arrangement of cryogenic capacitor and SFT detector. C_S is stray capacitance of C to ground, and R and R_S represent the leakage resistances of C and C_S respectively.

Figure 1 Cross-section through SiO capacitor. The diagram shows a cross-section of a capacitor assembly. It includes an SMD connector at the bottom, an end cap, a capacitor housing, evaporated gold electrodes, a fused quartz disc, another end cap, and a 23 mm wide section. The total height is 12 mm.

Figure 1 Cross-section through SiO capacitor

Figure 2 Cross-section through ³He-⁴He mixture capacitor



Sapphire was chosen in this case for its very low electrical conductivity. The capacitors were designed to have values of 1 pF, and after manufacturing were found to deviate from this nominal value by up to 20%. An Al-Al₂O₃ SFT was also mounted in the sample holder, and the gate electrode of the SFT was connected to one of the capacitor plates. The other plate was connected via a co-axial cable to a computer-controlled 16 bit DAC. A similar DAC controlled the SFT bias voltage, and the SFT current was measured with a low-noise current amplifier.

Experimental Method