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The cover design depicts the microwave planar near-field scanner being developed at NPL.

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A DC current source for metrology applications

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Introduction

This paper describes a circuit design for a DC current source for use in electrical metrology. The features of the design are a high output impedance, bipolar operation with grounded loads and a circuit stability and frequency response which are independent of the load impedance.

Theory of Operation

A simplified diagram of the current source is shown in figure 1.

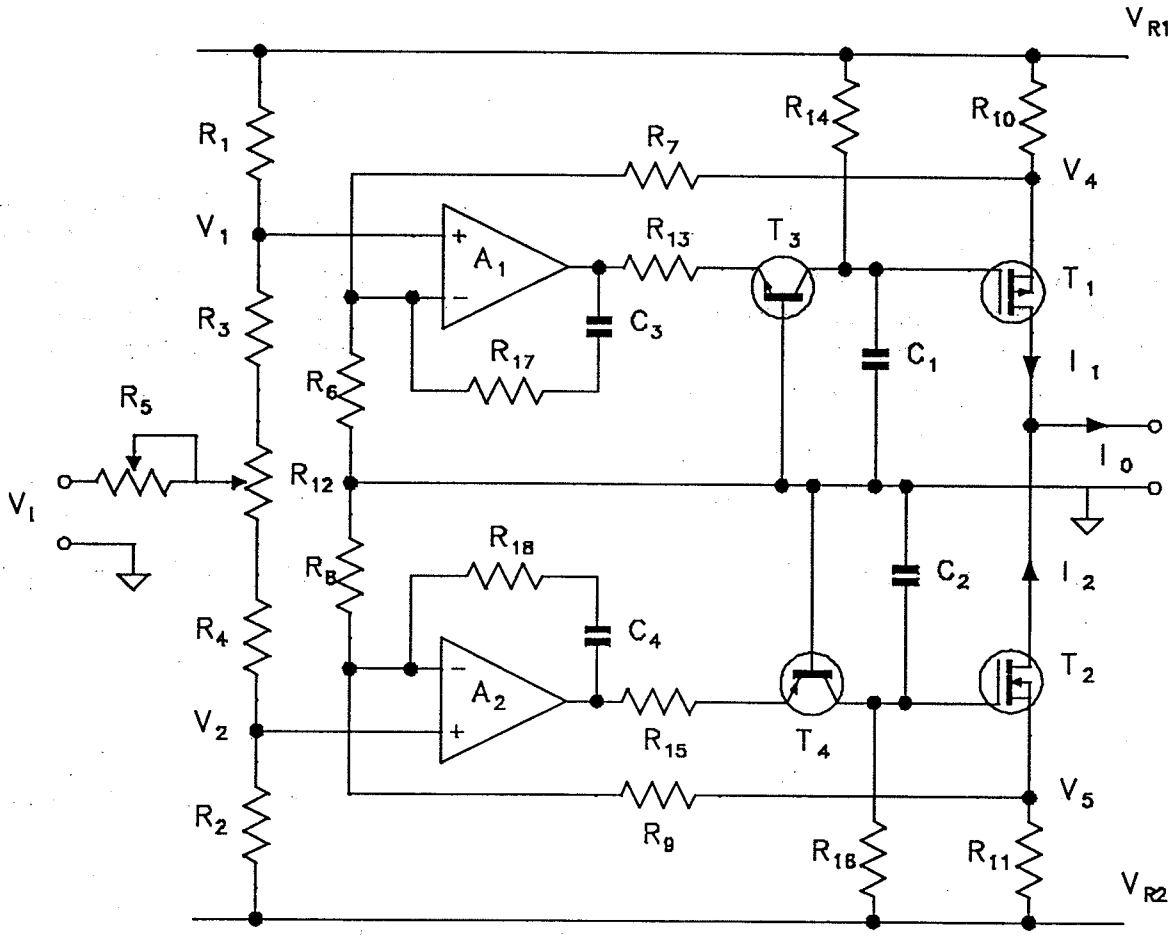

Figure 1

It utilises the high drain output impedance of a field effect transistor which is further enhanced by negative feedback of the voltage across a resistor in the source. The circuit consists of identical halves which operate in push-pull. Each half generates an output current and the two currents are summed at the output node. The output current is the difference between the two currents and is zero when they are equal and opposite.

The output current from the top half of the circuit is taken from the drain of the field effect transistor T_1 and is monitored by resistor R_{10} in the transistor source. The monitor voltage V_4 is fed back to the operational amplifier A_1. This amplifier aims to maintain the voltage V_4 according to the equation

$$V_4 = \frac{R_6 + R_7}{R_6} V_1 = G_1 V_1$$

and the output current from the stage, I_1, is given by

$$I_1 = \frac{V_{R1} - V_4}{R_{10}} = \frac{V_{R1} - G_1 V_1}{R_{10}}$$

where the current in the potential divider R_6+R_7 has been neglected. Similarly for the bottom half

$$I_2 = \frac{V_{R2} - V_5}{R_{11}} = \frac{V_{R2} - G_2 V_2}{R_{11}}$$

The currents I_1 and I_2 are dependent on the voltage of the power supply rails but the output current I_0=I_1+I_2 can be made independent of the rail voltages. This is achieved using the potential divider R_1 to R_5 which links the two halves of the circuit and provides the voltages V_1 and V_2. If the simplifying assumptions that R_1=R_2, R_3=R_4, G_1/R_{10}=G_2/R_{11}=G/R and that potentiometer R_{12} is set to its midpoint are made then it can be shown that the output current will be independent of changes in the supply rails if

$$R_5 = \frac{R_1 - R_3'(G-1)}{2(G-1)} \qquad where \qquad R_3' = R_3 + \frac{R_{12}}{2}$$

Under these conditions, the output current is related to the input voltage V_i by the simple expression

$$I_0 = \frac{-2(G-1)}{R} V_I$$

If the current taken by R_6 and R_7 is taken into account then R in the above expression becomes the parallel combination of R_{10} and R_6+R_7.

Circuit stability

One of the primary features of this circuit is that its frequency response and AC stability are virtually independent of the impedance of the load. This is because the negative feedback loop does not involve the load impedance and the only coupling between the output voltage developed across the load and the circuit is through the drain-gate capacitance C_{dg} in the output transistors. The effect of this coupling is reduced by the capacitors C_1 and C_2 which form a potential divider with C_{dg}. These capacitors introduce poles with time constants $R_{14}C_1$ and $R_{16}C_2$ into the negative feedback loops around A_1 and A_2 respectively and need to be

compensated by the networks R_{17} in series with C_3 and R_{18} in series with C_4 such that

$$R_{14}C_1 = (R_{17}+R_p)\,C_3 \qquad where \qquad R_p = \frac{R_6 R_7}{R_6+R_7}$$

and similarly for $R_{16}C_2$. The open loop gain is then characterised by two frequencies f_1 and f_2 where f_1 is the frequency at which the loop gain is unity, given by

$$f_1 = \frac{1}{2\pi C_3 R_7}$$

and f_2 is the -3 db frequency response of the operational amplifiers at a gain, G_{ac} , given by

$$G_{ac} = \frac{R_{17}+R_p}{R_p}$$

For the circuit to have a closed loop frequency response which is critically damped with a -3 db response of f_0 then f_1 and f_2 are chosen so that

$$f_0 = (f_1 f_2)^{1/2} \qquad with \qquad f_2 = 4 f_1$$

To obtain the largest value of C_1 and C_2 for a given value of f_0, the gain G_{ac} is chosen so that $f_2=2f_0$ and then f_2, C_3 and C_1 follow from above.

Practical details

The output stage is biased for class A operation with a quiescent current of just over half of the maximum required output current. The quiescent current (for the top half) is given by

$$I_Q = \frac{V_{R1}}{R_{10}}\left(1 - G\frac{R_3'}{R_1+R_3'}\right)$$

To obtain a reasonable compliance of the output voltage of the current source, the voltage across R_{10} should not be too large and a value of about 20% of the supply voltage is satisfactory.

To avoid the possibility of the circuit latching on switch-on, it is necessary to ensure that the voltages of the inverting inputs of the amplifiers are larger in magnitude than those of the non-inverting inputs when the output stage is turned off. This requirement places a minimum value on the resistance $R_6 + R_7$ which is given by the relation

$$I_Q(R_{10}+R_6+R_7) > V_{R1}$$

The value of $R_6 + R_7$ can be larger than the minimum given above but it should be noted that larger values will increase the overall noise of the circuit.

It is important that all of the output current from the output stage flows either through R_{10} or R_{11}. To ensure this, the output devices should either be field effect transistors or bipolar transistors with field effect transistors driving the base currents. The circuit gain and zero drift is affected by the resistors R_1 to R_{11} and so they should have a low temperature coefficient. In addition, R_{10} and R_{11} are required to handle the maximum output current.

The zero of the output current is set using the potentiometer R_{12} and the independence of the output current to the power supply voltages is achieved by adjusting R_5. The adjustment procedure is to set the current zero with equal and opposite supply voltages and then to vary one supply and adjust R_5 so that zero current is again obtained. Some iteration of these adjustments may be necessary.

Applications

The current source was designed for the NPL automated cryogenic current comparator bridge[1]. Here there is a requirement that the energising currents can be reversed in a continuous manner through zero and that the current source have good zero stability and linearity. In this application it is also important that the current sources have a well characterised frequency response as one of them forms part of a feedback loop.

There are many other possible applications for this current source design as the output current capacity is set only by the choice of the components in the output stage. So far, examples with maximum currents from 0.1 mA to 100 mA have been constructed but versions with higher output currents are feasible.

References

[1] Williams, J. M., and Hartland, A.: "An automated cryogenic current comparator resistance ratio bridge". *IEEE Trans. Instrum. Meas.*, 1991, **IM-40**, pp. 267-270