REVIEW ARTICLE | DECEMBER 01 2025

Classical interfaces for controlling cryogenic quantum computing technologies

Jack C. Brennan ; João Barbosa ; Chong Li ; Meraj Ahmad ; Fiheon Imroze ; Calum Rose ; Wridhdhisom Karar ; Manoj Stanley ; Hadi Heidari ; Nick M. Ridler ; Martin Weides

APL Quantum 2, 041501 (2025)
https://doi.org/10.1063/5.0273490

APL Quantum REVIEW pubs.aip.org/aip/apq

Classical interfaces for controlling cryogenic quantum computing technologies

Cite as: APL Quantum 2, 041501 (2025); doi: 10.1063/5.0273490
Submitted: 31 March 2025 • Accepted: 4 September 2025 •
Published Online: 1 December 2025

Jack C. Brennan,[1,a] João Barbosa,[1] Chong Li,[1] Meraj Ahmad,[1] Fiheon Imroze,[1] Calum Rose,[1] Wridhdhisom Karar,[1] Manoj Stanley,[2] Hadi Heidari,[1] Nick M. Ridler,[2] and Martin Weides[1,a]

AFFILIATIONS

[1] James Watt School of Engineering, University of Glasgow, Advanced Research Centre, Glasgow, G11 6EW Scotland, United Kingdom

[2] Electromagnetic & Electrochemical Technologies Department, National Physical Laboratory, Hampton Road, Teddington, TW11 0LW England, United Kingdom

[a] **Authors to whom correspondence should be addressed:** jack.brennan@glasgow.ac.uk and martin.weides@glasgow.ac.uk

ABSTRACT

Quantum processors have the potential to revolutionize computing on a scale unseen since the development of semiconductor technology in the middle of the twentieth century. However, while there is now huge activity and investment in the field, there are a number of challenges that must be overcome before the technology can be fully realized. Of primary concern is the development of the classical technology required to interface with quantum systems, as we push toward a new era of high-performance, large-scale quantum computing. In this review, we briefly discuss some of the main challenges facing the development of universally useful quantum computers and the different architectures being investigated. We are primarily concerned with cryogenic quantum systems. These systems are among the most mature quantum computing architectures to date and are garnering a lot of both industrial and academic attention. We present and analyze the leading methods of interfacing with quantum processors, both now and for the next generation of larger, multi-qubit systems. Recent advancements in control cryoelectronics, both semiconducting and superconducting, are covered, while a view toward newer methods such as optical and wireless qubit interfaces is also presented.

INTRODUCTION

Quantum computers have long been touted as the answer to ever-increasing demands for computing power, across a vast range of applications including cryptography, fundamental-physics research, and drug-discovery.[1–3] The attention and focus on quantum computing (QC) is accelerating as industrial, academic, and government organizations invest significantly in developing the technology and realizing its potential. While huge progress has been made in recent years,[4,5] there are important obstacles and issues to overcome before true *quantum advantage* is seen. A key area here concerns the quantum–classical interface needed to interact with and control the quantum processor.[6] Currently, within the noisy intermediate-scale quantum (NISQ) era,[7] quantum computers are limited to hundreds or potentially thousands of qubits, controlled by large numbers of cables and interconnects, and bulky, classical, electronic devices situated at various temperatures from cryogenic stages close to the qubit(s), right up to room temperature. The increasing space and cooling power requirements needed to sustain quantum-processing growth, in addition to the constant demand for fast, low-noise, high-fidelity electronics, makes tackling the issues surrounding the quantum–classical interface a high priority for the research field and industrial community. Here, we discuss the need to develop new or existing technologies and elucidate some of the current methods used.

ADVANCING AND SCALING UP THE NEXT GENERATION OF QUANTUM COMPUTERS

Scaling up the number of qubits comprising a quantum computer is a key aim of both industrial and academic researchers. The desire to move beyond the noisy intermediate-scale quantum

(NISQ) era of computing is evident throughout the industry, as seen by IBM's recent announcement to move toward a 100 000 physical-qubit system,[8] and the investments made by governments all over the world toward developing quantum information processors that outperform current, classical high-performance computers.[9,10] Scaling quantum computers to their full potential involves overcoming a series of complex challenges. This necessitates a collaborative approach, uniting the expertize of scientists, engineers, and industry. Despite significant progress,[11,12] there is still a considerable journey ahead. Central to this is engineering the appropriate classical interface for interacting with the quantum system. The primary challenges are listed in the following.

Quantum decoherence

Quantum systems are extremely sensitive to environmental disturbances, leading to a loss of coherence known as decoherence. As the number of qubits increases, the probability of errors due to decoherence also rises. Developing error-correction techniques and improving qubit stability are crucial for scaling up quantum computers.[13]

Qubit interactions and connectivity

Complex quantum systems require qubits to interact with each other to perform complex computations. As the number of qubits grows, maintaining and controlling the interactions between them becomes increasingly difficult. Ensuring high connectivity and minimizing unwanted interactions are essential for scaling up quantum computers.

Qubit quality and manufacturing

Quantum computers require high-quality qubits with low error rates. Current qubit technologies, such as superconducting circuits and trapped ions, face challenges in achieving consistently high qubit quality at scale. Improving fabrication techniques, reducing manufacturing defects, and optimizing qubit performance are critical for large-scale QC.[14]

Hardware scalability

Building a large-scale quantum computer requires integrating a massive number of qubits and other components into a coherent and controllable system. The physical infrastructure, including cryogenic cooling, wiring, and control systems, must be designed to accommodate the increasing complexity and size of the quantum processor. This challenge will be a focus of discussion within this review.

Quantum algorithms and error correction

Scaling up quantum computers requires developing robust error-correction codes capable of detecting and correcting errors introduced during computation. Designing efficient fault-tolerant quantum algorithms that can tolerate errors while still providing meaningful results is an ongoing research challenge.[15]

Programming and software tools

As quantum computers scale up, designing and implementing quantum algorithms become more complex.[16] Developing user-friendly programming languages, software libraries, and simulation tools to facilitate not just quantum software development and optimization but also the control systems for quantum hardware,[17] is crucial for wider adoption and efficient utilization of quantum computers.[18]

Cost and resources

Quantum computers are currently expensive to build and operate. While progress has been made, scaling up QC requires significant investments in research, development, and infrastructure. In addition, the demand for rare resources, such as high-quality qubit materials and specialized fabrication equipment, may pose supply chain challenges.

QUBIT ARCHITECTURES

The focus of this review concerns superconducting qubits, one of the leading platforms in developing quantum processors.[19] While other qubit architectures show promise in quantum information processing, many of these also require cryogenic conditions for operation, meaning the classical interfaces discussed herein are useful considerations across the field of QC. The main reasons for considering cryogenics are the need to establish the necessary physical operating conditions and for creating and maintaining a stable environment. Utilizing operating temperatures significantly below a material's superconducting energy gap (Δ) prevents random thermal excitations and enables Cooper pair formation for qubit realization. External interference coupled to the system, such as heat or electromagnetic radiation, can cause qubits to decohere; cryogenic temperatures significantly reduce this environmental noise. In practice, this dictates the maximum operational temperature, especially considering that qubit frequencies generally lie in the low GHz range, which necessitates an optimal temperature in the low mK regime.[20,21]

Superconducting qubits have been of interest for many years and are currently among the most widely used and heavily invested qubit types in QC research.[22,23] They are usually fabricated using multi-step additive and subtractive processes, involving lithographic patterning, metal deposition, wet/dry etching, and controlled oxidation of superconductor films. Reliable qubit fabrication at an industrial scale is still a major challenge and an active area of research for many.[24,25] Generally, materials such as aluminum or niobium are selected as the superconducting elements and these are patterned onto silicon or sapphire substrates.[26]

Superconducting qubits show great promise for several reasons, including their strong and relatively straightforward coupling to control signals, their relatively long and ever-increasing coherence times, and the clear path toward immediate scalability.[27] They must be operated at extremely low temperatures, typically around 10 s of mK inside dilution refrigerators, to both ensure the devices are far below the critical temperature (T_c) of the component material and to minimize the noise of the system.[26,28]

Quantum dot qubits utilize semiconductor nanostructures, known as quantum dots, to trap and manipulate single electrons as

qubits. They are typically fabricated using materials such as gallium arsenide or silicon, and operate at cryogenic temperatures, typically below 1 K.[29] Spin qubits utilize the intrinsic spin of electrons or nuclei in solid-state systems, such as quantum dots or defects in crystals such as nitrogen-vacancy (NV) centers in diamond. The cryogenic requirements for spin qubits can vary depending on the specific implementation. Some require operation at mK temperatures, while others can function at higher temperatures, around 1–4 K.[30]

Trapped ion qubits use individual ions, such as ytterbium or calcium. These ions are trapped and manipulated using electromagnetic fields in a vacuum chamber.[31] Photonic qubits use individual photons as qubits and manipulate them using various optical components such as beam splitters and detectors.[32,33] Cryogenic temperatures are not required for trapped ion or photonic qubits but can be beneficial in improving their operation.[34–36] For instance, some of the highest efficiency single-photon detectors, used to probe the state of a trapped ion or optical qubit, are based on superconducting materials that require Kelvin temperatures.[37–39]

The principles and proposed implementations of classical interfacing discussed here are relevant and potentially useful across many possible QC architectures.

INTERFACING WITH QUANTUM COMPUTERS

To access the computing power of a quantum system, the quantum state of a qubit must be manipulated, and it must be possible to generate and analyze any qubit state using the control and readout electronics. A major barrier to scaling up quantum computers stems from the room temperature electronics and optics needed to control and readout these quantum operations, placing limits on the signal bandwidth, latency, thermal load, and signal-to-noise ratio in the system. As quantum computers move to interacting systems of thousands of qubits, more room temperature electronics are required. There is a need to exploit the potential of information and communication technologies (ICT) as an interface to develop scalable, efficient integrated control and readout architectures.

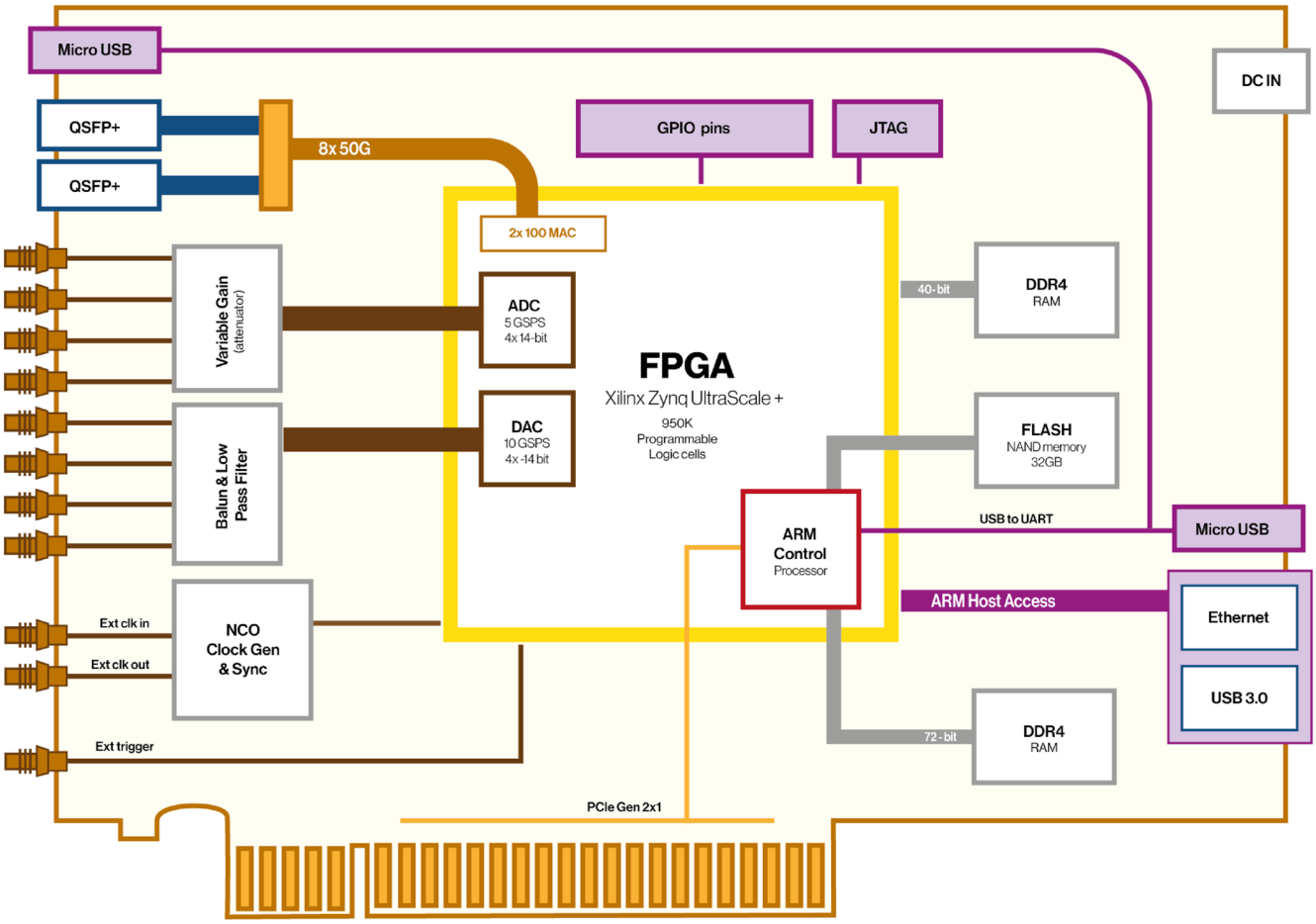

FIG. 1. Structural diagram of an integrated measurement device where the analog components are part of the integrated system on chip model architecture on a single integrated circuit board. The components are interacted through digital communication protocols through USB and Ethernet with a measurement PC.

Before the different interfacing approaches are discussed, it is important to highlight the major constraint in integrating technology within a cryogenic system: limited cooling power. For example, while a cryo-CMOS processor operating at just 77 K is predicted to achieve 3.4 times higher performance,[40] even cooling to this relatively high temperature can pose challenges. The 2022 IEEE international roadmap on *Cryogenic Electronics and Quantum Information Processing* lays out many of the opportunities and challenges associated with integrating cryogenic systems.[41] Of particular note for this work are the available cooling powers at various temperatures. At 4 K, for high powered cooling systems, there can be up to 1 kW of cooling power; however, at 20 mK, there is only up to 30 μW of cooling power. These cooling limits are currently placing restrictions on not only quantum processor size but also on the classical interfaces that can be placed within a cryostat.

CONVENTIONAL QUBIT CONTROL

A typical experimental setup involves two distinct microwave tones with similar properties, which pass through thermally anchored attenuator stages within a dilution refrigerator to suppress thermal noise before reaching the qubit sample. One of these signals is responsible for the control of the qubit state. By meticulously engineering various aspects of a microwave pulse, such as its amplitude, duration, and shape, it is possible to achieve any arbitrary state on the Bloch sphere within a timescale of tens of nanoseconds. An integrated measurement device is shown in Fig. 1, while a simplified schematic for conventional control and readout can be seen in Fig. 2. Advanced protocols with complex pulse sequences, such as the derivative removal by adiabatic gate or dynamical decoupling,[42,43] are further employed to reduce the unwanted side effects of anharmonicity and environment noise in real qubit devices, aiming to improving the fidelity of the control operation. These pulses are typically generated using a heterodyne scheme, where low-frequency signals from an arbitrary waveform generator (AWG) define the shape and duration of the pulse. These signals are then mixed with a high-frequency carrier signal near the qubit's fundamental transition frequency to produce the desired control waveform.

Another microwave tone is used to probe the qubit state in a dispersive readout architecture. After interacting with the qubit through the resonator on-chip, the tone is amplified at several stages and then mixed with the source-reference tone and finally converted from analog to digital and recorded for post-processing.[28] Each step induces noise, reducing the signal-to-noise ratio and improving each step individually is a major source of research and effort to

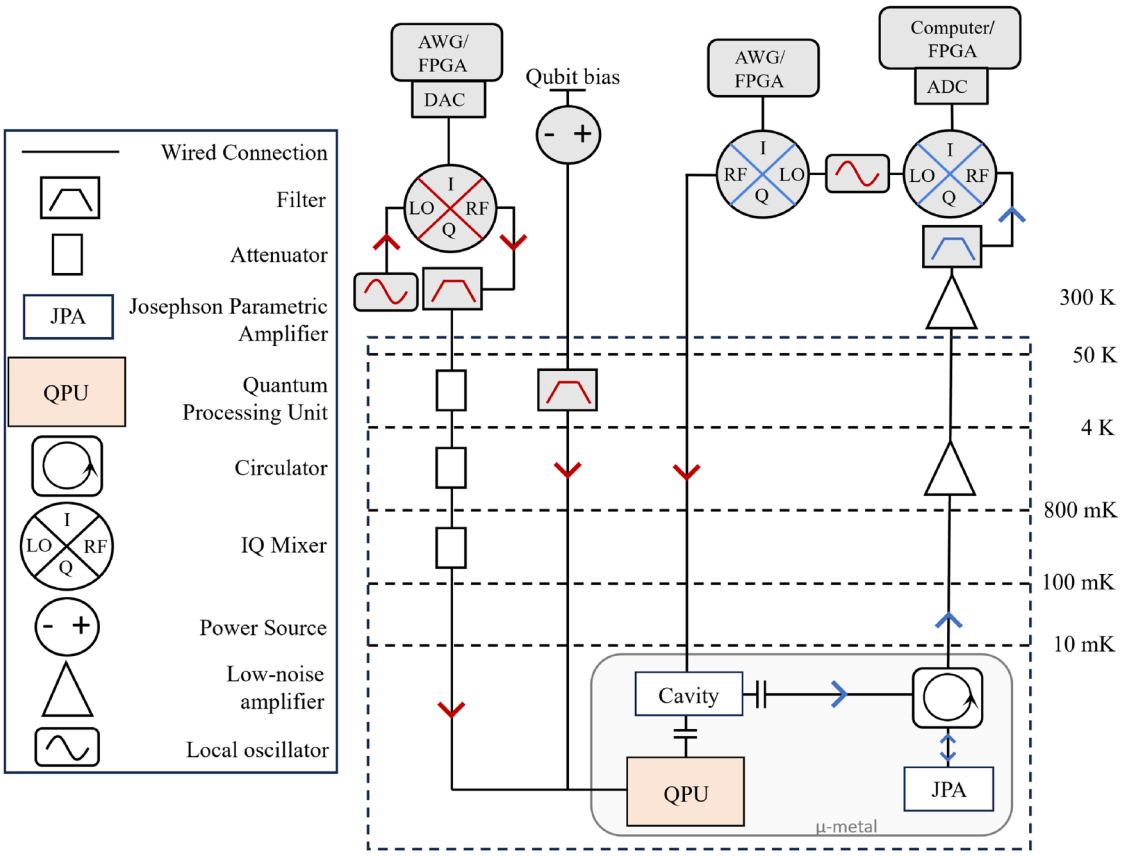

FIG. 2. Schematic outlining conventional control and readout of a superconducting transmon qubit within a dilution refrigerator.

enhance qubit control and readout. Inside the dilution refrigerator, the measurement chain includes circulators and isolators, to suppress backaction signals to the qubit,[44] and amplification through quantum-limited Josephson parametric amplifiers (JPA) and high-electron mobility transistor amplifiers.[22,45] Similar to the control tone, the probe tone performs a heterodyne/homodyne measurement, where a reference high-frequency carrier is mixed with a probe pulse from a digital to analog converter (DAC) or AWG to generate the readout tone by a process called upconversion.[46,47] After this, the transmission through signal is downconverted using the same reference carrier wave and recorded through an analog to digital converter (ADC). A major limitation stems from syncing all the individual drive electronics with an external clock, as they are usually generic and individually commercially sourced; this causes a delay ($\approx 1\ \mu s$), which significantly affects gate operations.

A modern hybrid approach involves field programmable gate arrays (FPGAs) based on custom hardware that combines an entire rack of generic microwave hardware on a single PCB with integrated chips performing dedicated drive and readout tasks. These components can be digitally programmed on FPGA fabric, for example, combining ADCs, DACs, filters, and attenuators on the same PCB, to record analog signals and decipher qubit states in real time. This enhances gate performance significantly and enables fast feedback control of multiple qubits in one go.[48] An Example FPGA board is shown in Fig. 1. Modern FPGA integrated circuits combine ADCs, DACs, and all other analog RF and digital components onto a single die fabric, incorporating a *System on Chip* philosophy to further reduce latency times between signal generation and readout to a few nanoseconds. The custom nature of these electronics enables these boards to be tailored to a quantum subsystem or generalized to perform an array of measurements from spectroscopy to multi-qubit control and sensor measurements.[49] Multiple commercial vendors have utilized this opportunity to produce customized products for quantum measurements, with a varied range of control/readout frequency ranges and high bitrate (up to 14-bit) analog signal capture.[50]

Overall, effectively reading out qubit systems at least requires high-speed classical electronics superseding qubit decay rates. Modern custom surface mount electronics coupled with FPGA/ASIC chips on board have been seen to be effective in multi-qubit control and readout. These classical electronics will need to keep improving, or new approaches will be required, as will be discussed here.

SCALING UP

Conventional approach

The scaling-up method currently being driven by large, industrial players in the field, Google and IBM, for example, revolves around simply increasing the number of control and readout lines, proportional to the number of qubits in the system. This necessitates a direct increase in the size of the cryostat and the cooling power required, with projects such as IBM's "Goldeneye" developing an mK cryostat on a previously unseen scale.[51] While this method has led to progress and may form the basis for the first generation of quantum computers, it is not a suitable long-term solution to the issue of scalability, as size and power requirements quickly become unreasonable for tens of thousands of qubits and above; this is particularly important amid a climate where power consumption is an important topic of research and discussion.[52,53]

Cryo-CMOS technologies

In a conventional QC setup, control and readout electronics, operating at room temperature, are typically positioned several meters away from the qubits. Conversely, the qubits are located in a cryogenic environment, maintaining temperatures in the tens of mK range. The signal latency, stemming from the length of the cables connecting the electronics to the qubits, results in a delay of hundreds of nanoseconds. This substantial latency proves unsuitable for fast quantum feedback measurements,[54] where the outcomes of single-shot qubit measurements immediately inform subsequent actions on the qubits. Reducing feedback latency is vital for minimizing error rates in the feedback operation and enhancing the overall fidelity of quantum information processing. Moreover, as the quantum system scales up by increasing the number of qubits, challenges mount due to the growing number of cable requirements. To effectively tackle these issues, relocating electronics to cryogenic temperatures (cryoelectronics) presents a potential solution, alleviating signal latency and many cable concerns.

Cryogenic electronics potentially empower rapid feedback mechanisms,[54] allowing for quick error correction[55,56] due to reduced feedback latency and ultimately enhancing the overall reliability of quantum computations while preserving the integrity of quantum information. In particular, cryogenic complementary metal–oxide semiconductor (cryo-CMOS) technologies have recently gathered significant attention from researchers due to their potential to revolutionize QC. Again, the distance between qubits at mK temperatures and the qubit readout and control circuitry operate at room temperature poses a significant problem that cryo-CMOS aims to overcome.[57–63] Cryo-CMOS technologies aim to address this issue by enabling the construction of custom-made readout and control circuitry that is designed to operate at cryogenic temperatures. A potential QC-cryo-CMOS architecture is presented in Fig. 3. However, specific challenges are associated with building such circuits, including power budget, noise, and bandwidth constraints.[64,65]

Two major technologies are currently being used in cryoelectronics QC hardware: bulk CMOS and fully depleted silicon-on-insulator (FDSOI).[66] Bulk CMOS technology, as in conventional CMOS technologies adapted to operate at cryogenic temperatures, offers low complexity and cost-effectiveness compared to FDSOI but poses several performance-related challenges when operated at cryogenic temperatures, such as carrier freeze-out, increased leakage current, kink effect, and hot carrier degradation.[67–71] FDSOI technology, on the other hand, is more sophisticated and offers greater benefits for cryogenic applications, including reduced leakage currents, low power consumption, and back biasing to counter threshold voltage shift at cryogenic temperatures.[72–74]

A critical aspect of advancing cryogenic CMOS technologies is the development of a cryogenic process design kit (PDK). This task involves characterizing devices at cryogenic temperatures as a first step. Room temperature data are verified from the foundry PDK if it falls within the process corners. The data are then calibrated at the desired cryogenic temperature using a technology computer aided design tool through reverse engineering.[75]

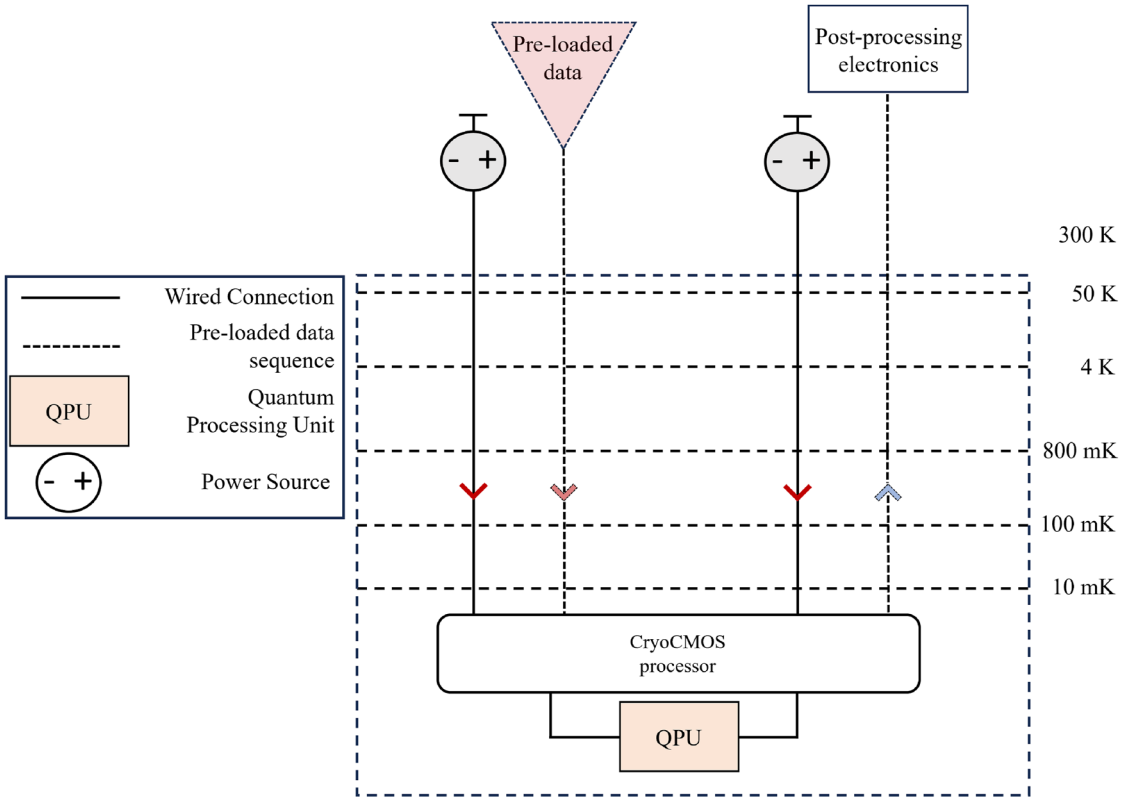

FIG. 3. Block diagram outlining the principle elements of a cryo-CMOS controlled superconducting qubit in a dilution refrigerator.

Compact model parameters are extracted, and the existing room temperature PDK is tuned to create a cryogenic PDK for that device.

While cryo-CMOS control potentially offers significant advantages for scaling QC, it does come with several limitations. One important constraint is the same issue conventional control has to tend with: when dealing with a large number of qubits, the number of control lines must still increase linearly.[64,65] One way to somewhat alleviate this issue would be to pre-load a data sequence into the cryo-CMOS processor in the cryostat. This would mean that only a power source would need to be connected to the cryo-CMOS processor through the cryostat and signals would not need to be sent in to the cryostat, from instruments outside the fridge, during measurements. However, there would still need to be many connections to the quantum processor. While these connections could be made using superconducting materials, below 4 K, to minimize the heat conduction between stages and electrical losses, the cryo-CMOS control circuits will still encounter issues with significant heat dissipation. This issue can potentially surpass the cooling capacity of the cryostat, resulting in an undesired increase in the qubit's temperature, disrupting all aspects of its operation.[76]

A review of the current state of research and development shows that prominent technology companies such as Google,[77] Intel,[78] and IBM[79] have played pivotal roles in advancing the integration of cryoelectronics to within the proximity of the qubit stage (4 K and below) by application specific integrated circuits (ASIC) using cryo-CMOS technologies. Indeed, the first European *Chips Joint Undertaking* project ARCTIC (Advanced Research on Cryogenic Technologies for Innovative Computing)[80] has started to establish a European supply chain for cryogenic quantum technologies, including cryogenic photonics, microelectronics, and cryo-microsystems to foster the low-cost, high-volume manufacturing of superconducting and semiconductor-based quantum chips in the EU.

What stands out as a remarkable achievement across these research efforts is the demonstration of practical control and readout architectures that function at cryogenic temperatures and exhibit high reliability and effectiveness, all with limited power dissipation. This concerted effort among these industry leaders underscores the significant strides in pursuing QC and quantum information processing technologies, with cryoelectronics serving as a critical enabler for advancing these QC applications. Overall, cryo-CMOS technology offers a potential solution to the scalability of quantum computers, provided a few implementation challenges are addressed. Initially, substantial effort is required to develop reliable cryogenic models that accurately replicate the cryogenic performance of CMOS circuits, before bespoke devices can be designed and fabrication processes can be initialized and industrialized.

Single flux quantum

Long-standing single flux quantum (SFQ) technology has recently been demonstrated to manipulate and control qubits in superconducting circuits.[81,82] This is a digital approach that utilizes the properties of superconducting materials, in the form of Josephson junctions, and the quantization of magnetic flux to encode and process quantum information.[83,84] An SFQ pulse is produced when magnetic flux through a superconducting circuit containing an overdamped Josephson junction changes by one flux quantum, Φ_0, as a result of the junction switching, which represents a 2π phase jump. SFQ pulses have a quantized area,

$$\int V(t)dt = \Phi_0 \approx 2.07 \cdot 10^{-15}\ \text{Wb} = 2.07\ \text{mV} \cdot \text{ps}. \quad (1)$$

Pulses can have a time interval as short as 1 ps, with an amplitude in the mV range, depending on the characteristic voltage of the circuit. In rapid single flux quantum (RSFQ) logic, one of the oldest and most developed logic families, propagating voltage pulses represent classical bits of information: the presence or absence of a voltage pulse across a Josephson junction in the circuit constitutes a classical 1 or 0 binary bit. Traditionally, RSFQ devices have been used in ultra-fast electronics, including ADCs, RF transceivers, and microprocessors, as it has long been possible to drive them to very high frequencies, with simple circuits shown to run at clock speeds of 770 GHz.[85]

An individual SFQ pulse produces a broadband excitation, so is incompatible with coherent manipulation of qubit systems, as specific qubit transitions cannot be isolated and excited.[86] Instead, the theory behind SFQ control of quantum systems relies on driving them using a train of SFQ pulses. The qubit is coherently excited using a pulse-to-pulse separation matched to its period.[87,88] As shown in Fig. 4, an external microwave tone is used to trigger a DC-SFQ converter, which generates the pulse train. The pulse train is then coupled capacitively to a transmon qubit, and each SFQ pulse induces an incremental rotation of the qubit state vector about the Bloch sphere. In this way, coherent and accurate qubit control can be achieved, with a predicted fidelity of >99.99%.[89] This has since theoretically been extended to multi-gate systems with promising results for maintaining high-fidelity control.[90] Experimentally, this approach has now been realized, with initial gate fidelities of ≈95%,[81] which have since been improved by redesigning the layout of the SFQ-qubit system using a multichip module.[82] The process of scaling up the number of qubits has now begun, with Bernhardt *et al.* reporting the first multi-qubit system integrating SFQ technology. Here, they utilize digital demultiplexing, breaking the linear scaling of control lines to number of qubits, showing promise for heat-load and space savings in cryogenic QC.[91]

SFQ-based qubit control is, therefore, a possible and promising avenue for qubit systems, but SFQ logic has also been touted for use in qubit readout. As discussed, superconducting qubits are generally measured using heterodyne detection of a coupled resonator, requiring significant equipment overhead throughout the cryostat and at room temperature for each qubit. A method has been presented by Opremcak *et al.*[92] and Howington *et al.*,[93] whereby a qubit state is mapped onto the photon occupation in a microwave cavity, after which the photon is detected using a Josephson photomultiplier (JPM), which effectively measures the qubit state and stores the result in a circulating current. An underdamped Josephson transmission line (JTL) coupled to the JPM delays or accelerates fluxons traveling along the JTL, depending on the circulating current in the JPM. The deviation in fluxon arrival time is converted to an SFQ logic signal, delivering digital qubit readout.

Another readout method has also been recently proposed, based on amplitude/phase discrimination of a microwave tone, whereby the phase of a coherent microwave tone can be probed between two distinct phase values by a device called Josephson digital phase detector (JDPD).[94] The JPDP can then be coupled to a qubit readout resonator and be able to distinguish between the two qubit states, which have a fixed phase difference due to the dispersive readout scheme. Interfacing the JPDP with SFQ electronics would be straightforward due to the nature of the device, creating an alternative way of fully digital readout of superconducting qubits.

An example of SFQ-qubit architecture is presented in Fig. 5. There are of course some drawbacks with implementing SFQ control and readout of qubit systems. A significant issue is the implementation and integration of SFQ devices into the commercially available dilution refrigerators commonly used for superconducting qubit research. The low-noise requirements and sensitivity of the devices to magnetic fields and trapped flux means that manageable, but not-insignificant, modifications are required to adapt the system from conventional qubit control architecture. In addition, quasiparticle

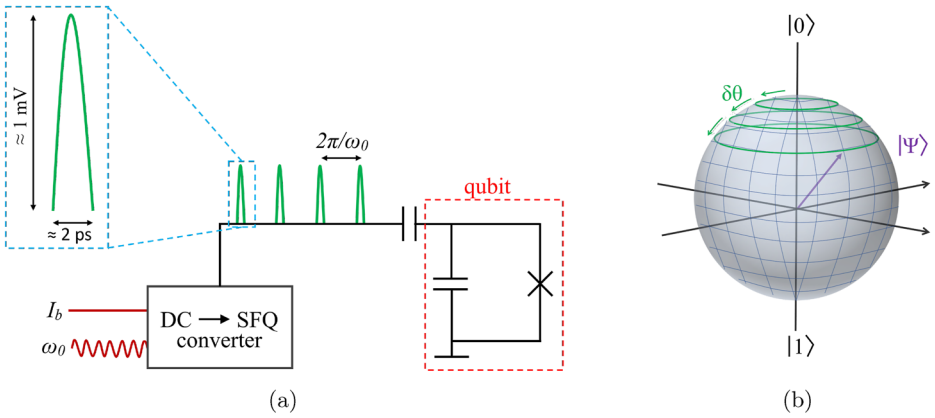

FIG. 4. Schematic for coherent qubit control based on a train of SFQ pulses. (a) In SFQ operation, a voltage pulse, with time integral quantized to Φ_0, is induced by a phase difference across a Josephson junction. A microwave signal of frequency ω_d is used to trigger a dc-SFQ converter, biased by a current I_b producing a train of pulses at $\frac{2\pi}{\omega_0}$ intervals, which is capacitively coupled to a transmon qubit. (b) Each SFQ pulse induces an incremental rotation of the qubit's state vector on the Bloch sphere.

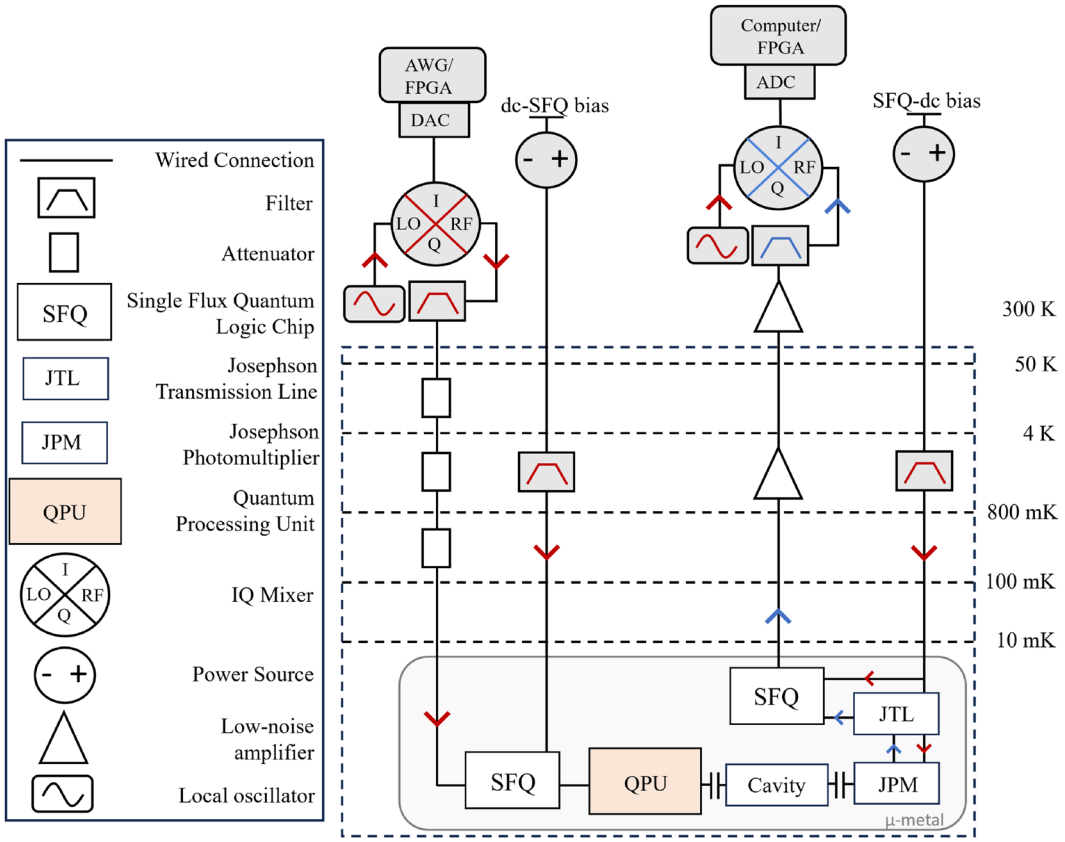

FIG. 5. Schematic showing the main elements of a control and readout architecture, for interfacing with superconducting qubits in a dilution refrigerator, using SFQ technology.

poisoning was seen to be an issue with early implementations of SFQ control. This has recently been improved significantly through installing the SFQ device at the 3 K cryostat stage[95] or implementing flipchip module architecture.[82] A useful overview of SFQ-quantum interface technologies can be found at Ref. 96.

Overall, SFQ technology is particularly well-suited for use in quantum computers due to its high speed, low energy consumption, and compatibility with existing superconducting circuitry. Modern energy efficient implementations of RSFQ (ERSFQ) devices can display a bit-switch energy of around 2×10^{-19} J with zero static power dissipation. In addition, adiabatic quantum-flux-parametron (AQFP) logic has emerged as a promising candidate for qubit control, offering even lower power dissipation due to its inherently reversible computational nature.[97] Even factoring in the energy cost of cryocooling the devices to below T_c, SFQ-based systems are projected to be more efficient than standard CMOS-based technologies for large scale computing.[53]

Optical control and readout

The potential for electro-optical technologies to be integrated with quantum devices is becoming an increasingly popular point of discussion. This is an area of research in which long-established techniques, in use globally for fiber-based information transmission, can be applied to the fields of QC and quantum sensing. The primary issue that can be addressed with electro-optical techniques is that of heat dissipation from coaxial cabling within the cryostat. The relevant technologies for enabling this technique will be discussed here alongside some examples of their use in cryogenic signal transmission applications; an example schematic can be seen in Fig. 6. The methods required for electro-optical signal transmission can be split into two main areas: encoding electrical signals onto the optical domain and recovery of the electrical signals. Encoding is generally carried out by an electro-optical modulator (EOM), which takes advantage of the Pockels effect in dielectric crystals.

This property can be exploited to control the optical path length of light propagating through the electro-optic crystal and in combination with optical waveguides, devices can be realized, which control the phase, intensity, and polarization of coherent light.[100] There are a range of metrics for quantifying EOM performance; when considering an EOM for use in cryogenic measurements, the location of the modulator will determine which metrics to prioritize. If an intensity modulator is to be used for encoding information on optical signals at room temperature, then a high extinction ratio (ER) is crucial. ER is the ratio between output in the modulators "on" state and "off" state; a high ER is desirable as it minimizes the

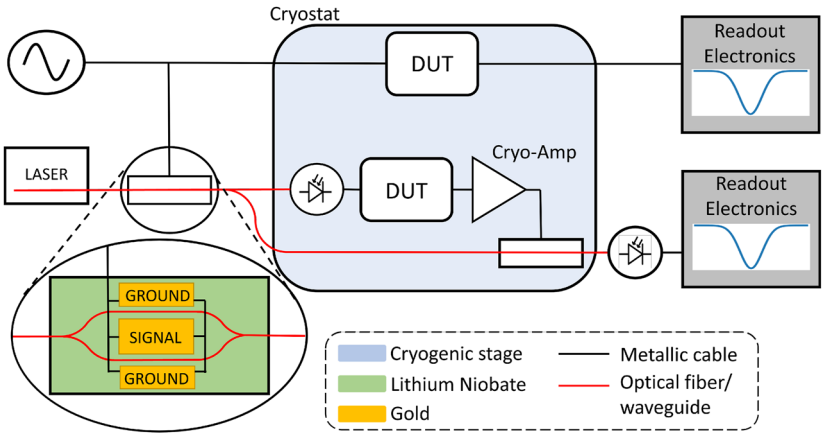

FIG. 6. Potential electro-optical control and readout method for superconducting devices based on work presented in Refs. 98 and 99. The top circuit shows a simplified model of conventional readout techniques using metallic cables, with the bottom diagram showing a method utilizing electro-optical components for transduction and optical fibers for signal transmission to cryogenic temperatures. The inset shows the design of an intensity modulator; the upper and lower waveguides cause an opposing increase and decrease in optical path length due to the opposite electric field in each arm, resulting in constructive and destructive interference at the output of the device.

laser power required to effectively transmit information. In practice, lithium niobate intensity modulators have been tested, with ERs upward of 20 dB.[101]

If the EOM is to be operated at cryogenic temperatures, other metrics must be taken into consideration, such as insertion losses, power consumption, and modulation efficiency. Insertion losses and power consumption both relate to the heat dissipated by the EOM in the cryogenic stage. Coupling of the optical fiber mode to the waveguide mode as well as dielectric losses will determine insertion losses, and the issue of coupling is complicated by the thermal stresses of cooling down to mK temperatures. It is not clear which approach to coupling works best but the work in Ref. 98 estimates that transmission of a device with glue bonds was reduced by 25% through the cooldown process. Power consumption is strongly related to electrode resistance, which can be greatly reduced by employing superconducting electrodes.[102]

Recovering an electrical signal from intensity modulated light is most simply carried out directly by a photodiode. If the optical signal is phase modulated, then an interferometer, such as a Mach–Zender interferometer, can be employed. Photodiodes are capable of detecting 1550 nm light at mK temperatures and can have a bandwidth of 10 s of GHz, which is suitable for current superconducting qubit measurements. Photodiodes have been demonstrated to provide shot-noise-limited performance in an electro-optical control scheme for qubits.[99] One drawback of commercially available photodiodes is the ubiquity of 50 Ω outputs lines. A photodiode with higher output impedance could achieve increased conversion gain, thus decreasing the laser power required.

The idea to use electro-optics to replace current cryogenic signals transmission techniques has gained some attention. In Ref. 99, the authors demonstrated low-noise qubit control and readout by replacing coaxial input lines with an electro-optical scheme. In Ref. 98, a superconducting electromechanical device was measured using a phase modulator at cryogenic temperatures to encode the signal. There has been some attention in the field of quantum sensing, with work carried out to control and readout superconducting single-photon detectors using electro-optical methods.[103,104] Recently, full readout of superconducting qubits has been shown by Arnold *et al.*, where they use radio-over-fiber down to mK temperatures, in an optical heterodyne detection scheme.[105] In this work, they show simultaneous upconversion and downconversion between microwave and optical frequencies, removing the requirement for any active or passive cryogenic microwave equipment. A low optical coupling efficiency means heat from the parametric pump being dumped at the mixing chamber, leading to temperature increase and some degradation of the qubit coherence. However, this setup has huge potential in reducing the heat-load and space needed inside the DR and lays out a path to meet the next round of engineering challenges to achieve qubit scale-up, as shown in Fig. 7.

Wireless control and readout

An alternative and recently studied solution is to implement wireless technology into QC systems.[106–110] Conventional wired connections for addressing and control of qubits can be directly replaced with wireless links.[106,107] Figure 8 illustrates a possible setup with separate control path (downlink, or DL) and readout path (uplink, or UL) inside the QC system. A reflection mode with DL and UL sharing the same optical path is also possible. The wireless links include transceivers and multiplexing units at both room temperature (RT) outside of the refrigerator and the mK stage inside the refrigerator, as well as beam control components including filters, and collimators or lenses linking the RT and mK transceivers. This technique has potentially many advantages over the state-of-the-art wired solutions.

1. All bulky and energy-hungry, but highly sophisticated and relatively mature, control and digital electronics remain at RT, making the cryostats much smaller, potentially leading to new and more compact designs where excitations and readouts via

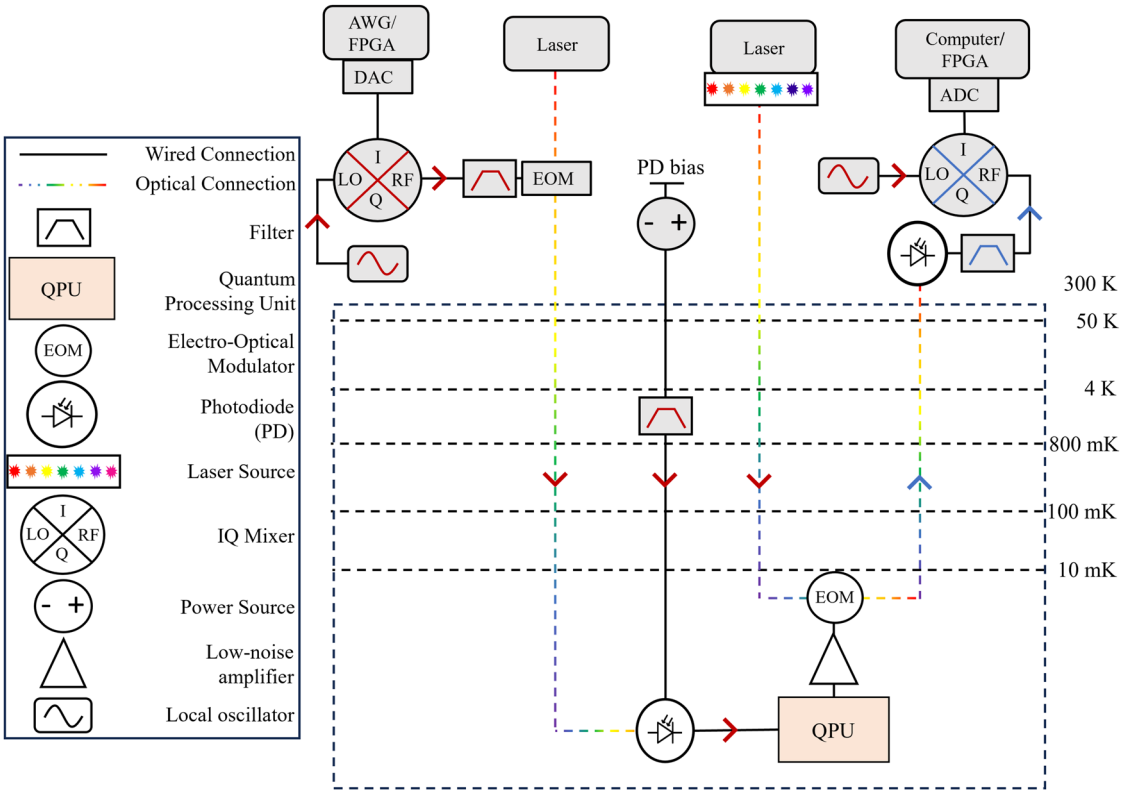

FIG. 7. Schematic showing the main elements of a proposed architecture for optically interfacing with superconducting qubits, within a dilution refrigerator.

side walls are possible, leaving the overall size of a QC only determined by the cooling system.

2. Wireless links can accommodate thousands or more channels (microwave tones with spacing of a few MHz subject to qubit technologies) co-existing, and therefore, qubit upscaling is no longer limited by the size of the refrigerator. In addition, many established wireless technologies such as channel coding and signal modulation can be implemented to improve control, robustness, resilience, and security.
3. Wireless links do not need a transmission medium; vacuum inside of the refrigerator makes signals propagate 33% faster than those in the coaxial cables. Thus, the latency between RT electronics and the qubits can be reduced by at least 33% and potentially more with shorter paths, which is crucial for high fidelity in many qubit technologies.
4. Thermal imbalance between the inner and outer conductors of the coaxial cables requires additional solutions, which increases overhead of QC systems. More importantly, the wired solutions bring excessive heat to the chamber, increasing the burden on the cryogenic cooling especially when the number of qubits rises to hundreds or more; on the contrary, the wireless solution has no such problems as there is no transmission loss in vacuum and the transceivers on the mK stage do not contain additional active devices but passives, such as antennas and matching circuits as well as qubit circuits. Since the passives could be realized by superconductors that have negligible ohmic loss at that stage, no extra power will be required apart from what is required by the qubits. Qubits' receiving antennae and multiplexing circuits could also be replaced by direct sensing with gate resonators in future developments.
5. There is much room for scalability to facilitate higher frequency signals. With millimeter wave frequencies, superconducting qubits could be operated at elevated temperatures, relaxing cooling power requirements, and higher processing frequencies. An example of this higher frequency operation has recently been shown by Anferov *et al.* for superconducting qubits.[111]

However, there are still many challenges including unknown signal propagation and scattering within the chambers, channel interferences and crosstalk, stray field associated noise on qubit performance, thermal control at the interfaces between ambient and the refrigerator and between chambers inside the refrigerator, realizing transceiver and multiplexing circuits for mK operations, and numerous unforeseen challenges from the diverse qubit technology. New cryogenic compatible microwave free space components are required, for example, antennas,[106] lenses,[107] etc.

An alternative wireless approach was proposed at MIT, which utilizes backscattering technology. In this approach, a CMOS transceiver chip is placed inside the fridge to receive and transmit data. Terahertz waves generated outside the refrigerator are beamed

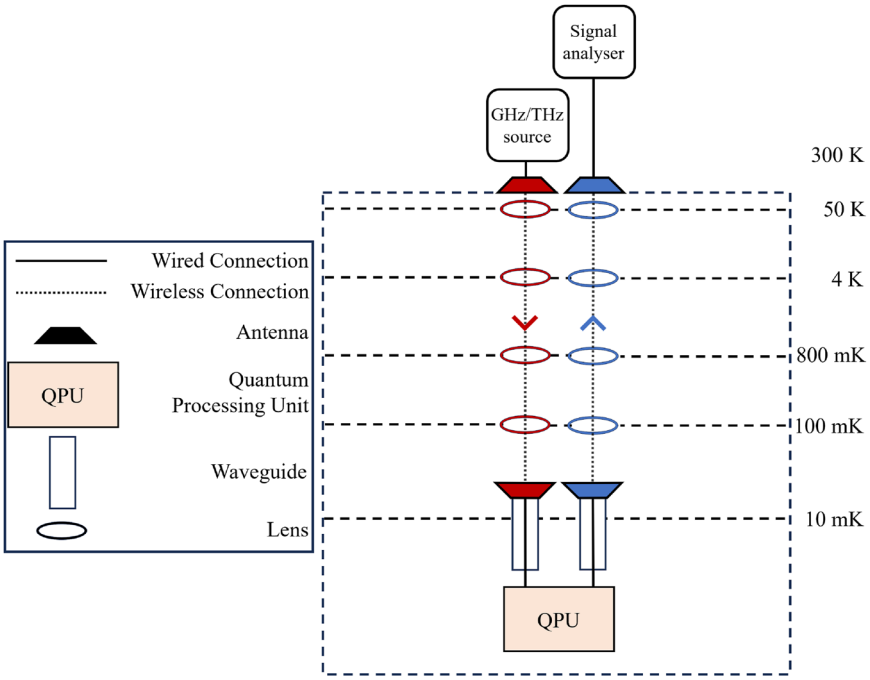

FIG. 8. Schematic showing an overview of the proposed wireless qubit control and readout architecture within a dilution refrigerator.

in through a glass window. Data encoded onto these waves can be received by the chip. This chip also acts as a mirror, delivering data from the qubits on the terahertz waves it reflects to their source. This reflection process also bounces back much of the power sent into the fridge, so the process generates only a minimal amount of heat. The contactless communication system consumes up to 10 times less power than systems with metal cables.[108,109] One of the challenges with this technology is that photon energy at THz is close to room temperature, and addressing how to reduce the impact of ambient temperature noise on these qubits is crucial. More recently, continuing the work, Wang *et al.* report the use of a wireless terahertz cryogenic interconnect combined with cryo-CMOS technology.[112] Wideband transceivers with a carrier frequency of 260 GHz, a hot-to-cold ingress based on passive cold field-effect transistor terahertz detector, and a cold-to-hot egress using ultralow-power backscatter modulation at the cold reservoir define this system, where they show that the ratio of information transfer to thermal heat transfer approaches the fundamental limit of what an equivalent optical interconnect can achieve. Again, they set out a path to the next stage of engineering problems needing to be solved to allow wireless scaling of multi-qubit systems.

Power and scalability considerations

To evaluate the potential of different technologies for use in future large-scale systems, it is essential to consider several key metrics. Table I highlights the most relevant metrics for scaling superconducting quantum computing platforms beyond the NISQ

TABLE I. Comparison of classical interfaces with respect to scalability and power consumption.

Technology	No. of Drive and readout lines	No. of Flux lines	Controller-qubit distance	Power consumption per physical qubit
Standard microwave	5–200/100 qubits[a]	1/qubit	RT-mK	>1 W[63]
Cryo-CMOS	5–200/100 qubits[a]	1/qubit	4K/mK-mK[b]	2–30 mW[53,63]
SFQ logic	None[c]	None[c]	mK-mK	<1 nW[82,96]
Optical	None[d]	1/qubit	RT-mK	<10 nW (Optical-RF)[98] <10 μW (RF-Optical)[99,113]
Wireless	None	0.5/qubit[e]	RT-mK	<1 nW

[a]Assuming an optimal control and readout multiplexing scheme,[53] and a worst case of a single control and readout line per qubit.
[b]The goal of much cryo-CMOS research is to implement systems as close as possible to the QPU, i.e., mK,[114] but it is likely that early implementations will be at 4 K due to volume and cooling requirements.
[c]Assuming an integrated SFQ-qubit approach with capacitive and inductive couplings between the two elements.[81,82]
[d]Drive and readout lines replaced with optical fibers.
[e]Provided polarization and (or) modulation schemes are applied.

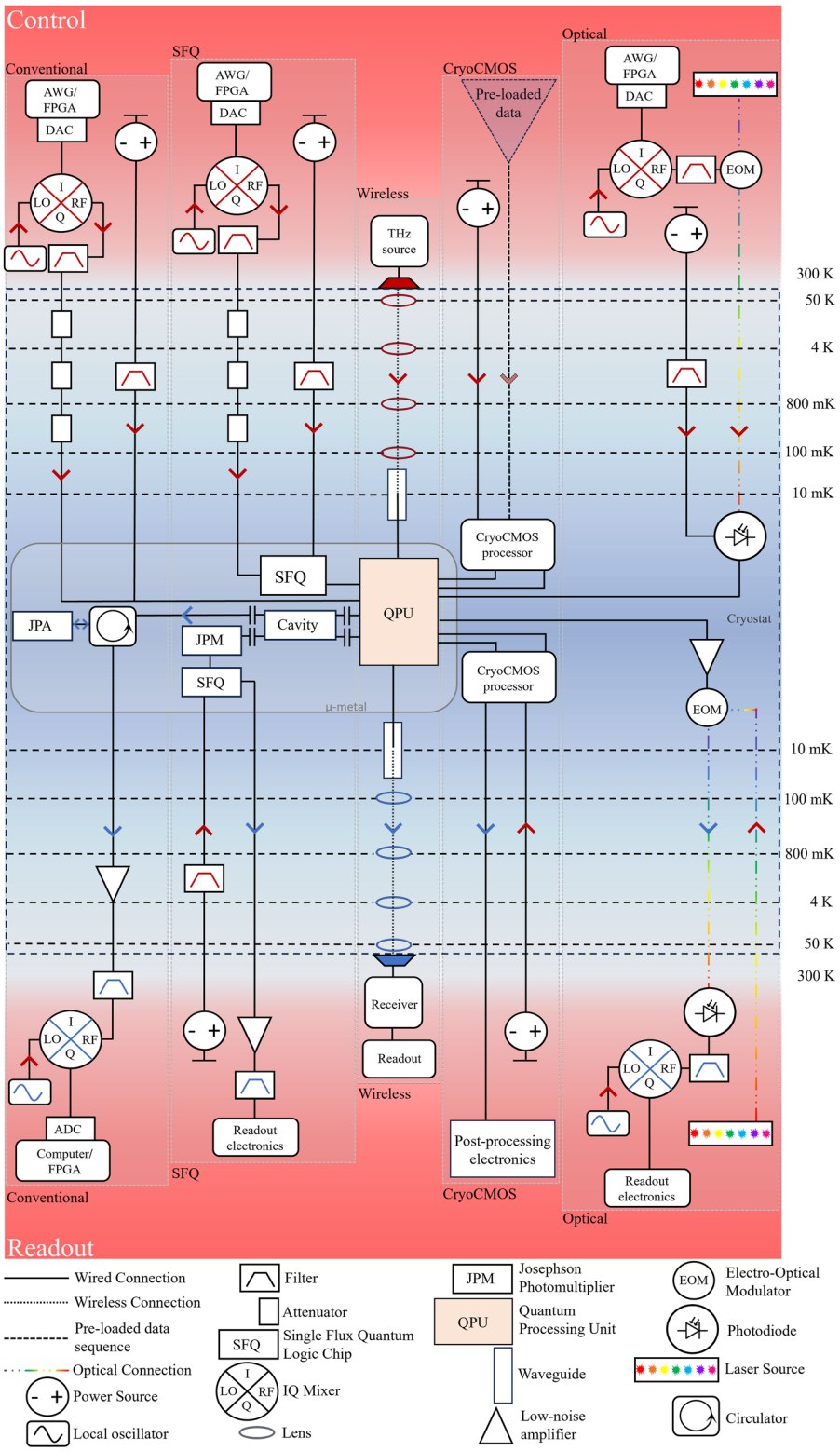

FIG. 9. Simplified wiring schematics of leading control (top) and readout (bottom) architectures for superconducting quantum processing units (QPUs). From left to right: conventional, single flux quantum (SFQ), wireless, CryoCMOS, and optical interfaces.

era. These include the number of coaxial lines, such as drive, readout, and flux lines, connecting the controller units to the physical qubits inside the cryostat, the physical separation between these components across the stages of a conventional dilution refrigerator, and an estimation of the power consumption required to operate a single physical qubit effectively.

The number of physical wiring lines within the cryostat is a critical consideration as the number of qubits scales up. The internal volume and cooling power of a cryostat place a hard limit on the number of wires, particularly coaxials, which can be used. Subsequently, any future control system based on physical wiring will probably require multiplexing architectures.[114,115] The most common of these is a frequency multiplexing system, where a single line is used to encode signals with multiple frequencies, each targeting a certain component of the qubit array. Based on Ref. 53, the values shown in Table I for conventional and cryo-CMOS technologies present an optimistic multiplexed control and readout architecture. This features 100:1 readout resonator multiplexing, corresponding to a 10 MHz separation within a 1 GHz bandwidth, and a 25:1 multiplexing of control lines, corresponding to a 50 MHz distancing within a 1 GHz bandwidth. In practical near-term quantum systems, the best readout multiplexing ratios decrease to 8:1, as seen in IBM's quantum processors.[116] This limitation arises from the constrained bandwidth of quantum-limited parametric amplifiers, which restrict the number of frequency-multiplexed signals that can be amplified simultaneously. In addition, each qubit requires a dedicated control line due to the low anharmonicity of transmon qubits, which prevents effective multiplexing for control signals. For flux-tunable qubit architectures, an additional flux line is required per qubit to enable frequency tuning and enable the execution of some single-qubit and two-qubit gates.

In the case of the remaining technologies, all the drive and readout wiring between the controlling unit and the qubit chip is removed, facilitating a scaling up of the number of qubits. Flux lines might still be needed, as is the case for wireless technologies since these cannot be used in conjunction with the DC signals required to tune qubits to their optimal frequency. Nevertheless, using polarization or modulation schemes with the wireless signals, it is potentially possible to address more than one qubit with the same biasing conditions, reducing the overhead further. SFQ logic controllers, in particular, are the only technology in this review that can be used on the mK stage of the cryostat, in close proximity to the qubit chip. This means that all the wiring between these two units can be completely removed, and simple capacitive and inductive connections, either via flip-chip modules or with both units fabricated on the same substrate, facilitate the interaction between them.[81,82]

Another critical metric is the power consumption required to operate a single qubit,[53] which encompasses not only the signals themselves but also the energy demands of the supporting electronic systems. Particularly for CMOS technologies, the values shown in Table I indicate the total AC and DC power provided to an FPGA and RF module to generate a stream of control pulses at a frequency around 1 GHz.[63] The power requirements can vary dramatically across different technologies, but their impact also depends significantly on the temperature stage at which the electronics are located. For instance, while room-temperature electronics dissipate substantial heat, their scalability is practically unconstrained by thermal considerations. In contrast, cryo-CMOS electronics operating at the 4 K stage must adhere to stringent cooling power limitations to ensure proper functionality, as the available cooling power diminishes with decreasing temperature. In the case of SFQ logic and because of the superconducting nature of these circuits, the power dissipated is given solely by the dynamical switching of the Josephson junctions and is proportional to their critical current and the frequency of operation.[86,96] Optical links remove the need for coaxial wiring and attenuators along the control lines, instead replacing it with simple and efficient optical fibers. Here, the majority of energy losses occur during the conversion between the optical and RF domains, with the RF-to-optical conversion being particularly inefficient. For instance, using a projected performance of $V_\pi = 50$ mV, insertion loss of 2.5 dB per facet, and waveguide loss of 0.05 dB/cm,[113] the power dissipation is in the order of tens of μW per qubit. In comparison, optical-to-RF photodiode conversion achieves power dissipation in the nW range under similar conditions. Both scenarios assume a 1% duty cycle, where the laser is active only during qubit addressing. Wireless technology also removes the need of attenuators in the drive lines, allowing the usage of much lower power microwave circuitry, which are able to generate and transmit single photon power signals directly from on-chip antennas.

CONCLUSION

We have reviewed the current state of the art in terms of the classical interfaces required to control cryogenic quantum systems. A larger schematic, giving a simplified overview of each of these potential interfaces, is shown in Fig. 9. Given the unique strengths and limitations of each technology, it is likely that future large-scale quantum devices will leverage a combination of these technologies, strategically applied at different stages of the setup to maximize their respective advantages. Quantum devices have huge potential across a number of fields and could represent a paradigm shift in many areas of technology. However, control systems for these devices are currently at a very early stage of development and progress needs to be made to keep up with the rapid advances in areas such as qubit fabrication and quantum algorithms or software.

ACKNOWLEDGMENTS

This work was supported by the EPSRC QCS Hub (PRF-02-A-03), UKRI Innovate UK Cryo-CMOS to enable scalable quantum computers project (Grant No. 10006017), UKRI Innovate UK Altnaharra: Cryoelectronics for Quantum Circuits project (Grant No. 10006186), UKRI EPSRC Empowering Practical Interfacing of Quantum Computing (EPIQC) (Grant No. EP/W032627/1), and EPSRC under Grant No. EP/X017613/1.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jack C. Brennan: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Project administration (lead); Writing –

original draft (lead); Writing – review & editing (lead). **João Barbosa**: Data curation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Chong Li**: Data curation (equal); Funding acquisition (lead); Writing – original draft (supporting). **Meraj Ahmad**: Data curation (supporting). **Fiheon Imroze**: Data curation (supporting). **Calum Rose**: Data curation (supporting); Writing – original draft (supporting). **Wridhdhisom Karar**: Writing – original draft (supporting). **Manoj Stanley**: Writing – review & editing (supporting). **Hadi Heidari**: Data curation (supporting). **Nick M. Ridler**: Writing – review & editing (supporting). **Martin Weides**: Conceptualization (equal); Funding acquisition (lead); Project administration (equal); Writing – original draft (supporting); Writing – review & editing (supporting).

DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

REFERENCES

[1] A. Steane, "Quantum computing," Rep. Prog. Phys. **61**, 117 (1998).
[2] P. Spentzouris, *Quantum Computing: Advancing Fundamental Physics* (Springer, 2020).
[3] *The Future of Drug Development with Quantum Computing*, edited by B. Bonde, P. Patil, B. Choubey, and A. Heifetz (Springer, 2024), pp. 153–179.
[4] E. R. MacQuarrie, C. Simon, S. Simmons, and E. Maine, "The emerging commercial landscape of quantum computing," Nat. Rev. Phys. **2**, 596–598 (2020).
[5] A. K. Fedorov, N. Gisin, S. M. Beloussov, and A. I. Lvovsky, "Quantum computing at the quantum advantage threshold: A down-to-business review," arXiv:2203.17181 (2022).
[6] C. G. Almudever, L. Lao, X. Fu, N. Khammassi, I. Ashraf, D. Iorga, S. Varsamopoulos, C. Eichler, A. Wallraff, L. Geck, A. Kruth, J. Knoch, H. Bluhm, and K. Bertels, "The engineering challenges in quantum computing," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017, Lausanne, Switzerland, 27–31 March 2017* (IEEE, 2017), pp. 836–845.
[7] J. Preskill, "Quantum computing in the NISQ era and beyond," Quantum **2**, 79 (2018).
[8] IBM: IBM: Charting the course to 100,000 qubits, https://research.ibm.com/blog/100k-qubit-supercomputer, 2023.
[9] UK Department for Science, Innovation, and technology: UK government: National quantum strategy, 2023, https://www.gov.uk/government/publications/national-quantum-strategy.
[10] European Commission: EU, Quantum technologies flagship, 2022, https://digital-strategy.ec.europa.eu/en/policies/quantum-technologies-flagship.
[11] S. S. Gill, A. Kumar, H. Singh, M. Singh, K. Kaur, M. Usman, and R. Buyya, "Quantum computing: A taxonomy, systematic review and future directions," Software: Pract. Exp. **52**, 66–114 (2022).
[12] National Academies of Sciences, *Engineering, and Medicine: Quantum Computing: Progress and Prospects* (National Academies Press, Washington, DC, 2019), https://nap.nationalacademies.org/catalog/25196/quantum-computing-progress-and-prospects.
[13] I. Siddiqi, "Engineering high-coherence superconducting qubits," Nat. Rev. Mater. **6**, 875–891 (2021).
[14] N. P. de Leon, K. M. Itoh, D. Kim, K. K. Mehta, T. E. Northup, H. Paik, B. S. Palmer, N. Samarth, S. Sangtawesin, and D. W. Steuerman, "Materials challenges and opportunities for quantum computing hardware," Science **372**(6539), 2823 (2021).
[15] E. Campbell, "A series of fast-paced advances in quantum error correction," Nat. Rev. Phys. **6**, 160–161 (2024).
[16] K. Bharti, A. Cervera-Lierta, T. H. Kyaw, T. Haug, S. Alperin-Lea, A. Anand, M. Degroote, H. Heimonen, J. S. Kottmann, T. Menke, W.-K. Mok, S. Sim, L.-C. Kwek, and A. Aspuru-Guzik, "Noisy intermediate-scale quantum algorithms," Rev. Mod. Phys. **94**, 015004 (2022).
[17] N. Shammah, A. Saha Roy, C. G. Almudever, S. Bourdeauducq, A. Butko, G. Cancelo, S. M. Clark, J. Heinsoo, L. Henriet, G. Huang, C. Jurczak, J. Kotilahti, A. Landra, R. LaRose, A. Mari, K. Nowrouzi, C. Ockeloen-Korppi, G. Prawiroatmodjo, I. Siddiqi, and W. J. Zeng, "Open hardware solutions in quantum technology," APL Quantum **1**(1), 011501 (2024).
[18] M. Cerezo, A. Arrasmith, R. Babbush, S. C. Benjamin, S. Endo, K. Fujii, J. R. McClean, K. Mitarai, X. Yuan, L. Cincio, and P. J. Coles, "Variational quantum algorithms," Nat. Rev. Phys. **3**, 625–644 (2021).
[19] O. Ezratty, "Perspective on superconducting qubit quantum computing," Eur. Phys. J. A **59**, 94 (2023).
[20] K. Serniak, M. Hays, G. de Lange, S. Diamond, S. Shankar, L. D. Burkhart, L. Frunzio, M. Houzet, and M. H. Devoret, "Hot nonequilibrium quasiparticles in transmon qubits," Phys. Rev. Lett. **121**, 157701 (2018).
[21] S. Krinner, S. Storz, P. Kurpiers, P. Magnard, J. Heinsoo, R. Keller, J. Lütolf, C. Eichler, and A. Wallraff, "Engineering cryogenic setups for 100-qubit scale superconducting circuit systems," EPJ Quantum Technol. **6**(1), 2 (2019).
[22] J. Clarke and F. K. Wilhelm, "Superconducting quantum bits," Nature **453**(7198), 1031–1042 (2008).
[23] G. Wendin, "Quantum information processing with superconducting circuits: A review," Rep. Prog. Phys. **80**, 106001 (2017).
[24] J. Verjauw, R. Acharya, J. V. Damme, T. Ivanov, D. P. Lozano, F. A. Mohiyaddin, D. Wan, J. Jussot, A. M. Vadiraj, M. Mongillo, M. Heyns, I. Radu, B. Govoreanu, and A. Potočnik, "Path toward manufacturable superconducting qubits with relaxation times exceeding 0.1 ms," npj Quantum Inf. **8**, 93 (2022).
[25] J. Van Damme, S. Massar, R. Acharya, T. Ivanov, D. Perez Lozano, Y. Canvel, M. Demarets, D. Vangoidsenhoven, Y. Hermans, J. G. Lai, A. M. Vadiraj, M. Mongillo, D. Wan, J. De Boeck, A. Potočnik, and K. De Greve, "Advanced cmos manufacturing of superconducting qubits on 300 mm wafers," Nature **634**(8032), 74–79 (2024).
[26] M. Kjaergaard, M. E. Schwartz, J. Braumüller, P. Krantz, J. I.-J. Wang, S. Gustavsson, and W. D. Oliver, "Superconducting qubits: Current state of play," Annu. Rev. Condens. Matter Phys. **11**, 369 (2020).
[27] W. D. Oliver and P. B. Welander, "Materials in superconducting quantum bits," MRS Bull. **38**, 816–825 (2013).
[28] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver, "A quantum engineer's guide to superconducting qubits," Appl. Phys. Rev. **6**(2), 021318 (2019).
[29] S. G. J. Philips, M. T. Mądzik, S. V. Amitonov, S. L. de Snoo, M. Russ, N. Kalhor, C. Volk, W. I. L. Lawrie, D. Brousse, L. Tryputen, B. P. Wuetz, A. Sammak, M. Veldhorst, G. Scappucci, and L. M. K. Vandersypen, "Universal control of a six-qubit quantum processor in silicon," Nature **609**(7929), 919–924 (2022).
[30] G. Burkard, T. D. Ladd, A. Pan, J. M. Nichol, and J. R. Petta, "Semiconductor spin qubits," Rev. Mod. Phys. **95**(2), 025003 (2023).
[31] C. D. Bruzewicz, J. Chiaverini, R. McConnell, and J. M. Sage, "Trapped-ion quantum computing: Progress and challenges," Appl. Phys. Rev. **6**(2), 021314 (2019).
[32] S. Slussarenko and G. J. Pryde, *Photonic Quantum Information Processing: A Concise Review* (American Institute of Physics, Inc., 2019).
[33] R. K. Ramakrishnan, A. B. Ravichandran, A. Mishra, A. Kaushalram, G. Hegde, S. Talabattula, and P. P. Rohde, "Integrated photonic platforms for quantum technology: A review," ISSS J. Micro Smart Syst. **12**(2), 83–104 (2023).
[34] M. F. Brandl, M. W. van Mourik, L. Postler, A. Nolf, K. Lakhmanskiy, R. R. Paiva, S. Möller, N. Daniilidis, H. Häffner, V. Kaushal, T. Ruster, C. Warschburger, H. Kaufmann, U. G. Poschinger, F. Schmidt-Kaler, P. Schindler, T. Monz, and R. Blatt, "Cryogenic setup for trapped ion quantum computing," Rev. Sci. Instrum. **87**, 113103 (2016).
[35] G. Pagano, P. W. Hess, H. B. Kaplan, W. L. Tan, P. Richerme, P. Becker, A. Kyprianidis, J. Zhang, E. Birckelbaw, M. R. Hernandez, Y. Wu, and C. Monroe, "Cryogenic trapped-ion system for large scale quantum simulation," Quantum Sci. Technol. **4**, 014004 (2018).
[36] K. R. Brown, J. Chiaverini, J. M. Sage, and H. Häffner, "Materials challenges for trapped-ion quantum computers," Nat. Rev. Mater. **6**, 892–905 (2021).
[37] S. L. Todaro, V. B. Verma, K. C. McCormick, D. T. C. Allcock, R. P. Mirin, D. J. Wineland, S. W. Nam, A. C. Wilson, D. Leibfried, and D. H. Slichter, "State readout of a trapped ion qubit using a trap-integrated superconducting photon detector," Phys. Rev. Lett. **126**, 010501 (2021).

[38]S. Gyger, J. Zichi, L. Schweickert, A. W. Elshaari, S. Steinhauer, S. F. Covre da Silva, A. Rastelli, V. Zwiller, K. D. Jöns, and C. Errando-Herranz, "Reconfigurable photonics with on-chip single-photon detectors," Nat. Commun. **12**, 1408 (2021).
[39]I. Esmaeil Zadeh, J. Chang, J. W. N. Los, S. Gyger, A. W. Elshaari, S. Steinhauer, S. N. Dorenbos, and V. Zwiller, "Superconducting nanowire single-photon detectors: A perspective on evolution, state-of-the-art, future developments, and applications," Appl. Phys. Lett. **118**(19), 190502 (2021).
[40]I. Byun, D. Min, G. Lee, S. Na, and J. Kim, "A next-generation cryogenic processor architecture," IEEE Micro **41**(3), 80–86 (2021).
[41]D. Holmes, "Cryogenic electronics and quantum information processing," in *2021 IEEE International Roadmap for Devices and Systems Outbriefs* (IEEE Computer Society, Los Alamitos, CA, 2021), pp. 1–93.
[42]F. Motzoi, J. M. Gambetta, P. Rebentrost, and F. K. Wilhelm, "Simple pulses for elimination of leakage in weakly nonlinear qubits," Phys. Rev. Lett. **103**, 110501 (2009).
[43]N. Ezzell, B. Pokharel, L. Tewala, G. Quiroz, and D. A. Lidar, "Dynamical decoupling for superconducting qubits: A performance survey," Phys. Rev. Appl. **20**, 064027 (2023).
[44]D. M. Pozar, *Microwave Engineering*, 4th ed. (John Wiley & Sons, Inc, Hoboken, 2011).
[45]C. M. Caves, "Quantum limits on noise in linear amplifiers," Phys. Rev. D **26**(8), 1817–1839 (1982).
[46]U. Leonhardt and H. Paul, "Realistic optical homodyne measurements and quasiprobability distributions," Phys. Rev. A **48**(6), 4598 (1993).
[47]H. M. Wiseman and G. J. Milburn, *Quantum Measurement and Control* (Cambridge University Press, (2009), https://www.cambridge.org/core/product/identifier/9780511813948/type/book.
[48]Y. Salathé, P. Kurpiers, T. Karg, C. Lang, C. K. Andersen, A. Akin, S. Krinner, C. Eichler, and A. Wallraff, "Low-latency digital signal processing for feedback and feedforward in quantum computing and communication," Phys. Rev. Appl. **9**(3), 034011 (2018).
[49]L. Stefanazzi, K. Treptow, N. Wilcer, C. Stoughton, C. Bradford, S. Uemura, S. Zorzetti, S. Montella, G. Cancelo, S. Sussman, A. Houck, S. Saxena, H. Arnaldi, A. Agrawal, H. Zhang, C. Ding, and D. I. Schuster, "The QICK (quantum instrumentation control kit): Readout and control for qubits and detectors," Rev. Sci. Instrum. **93**(4), 044709 (2022).
[50]Quantum machines: OPX+: Ultra-fast quantum control hardware, 2023, https://www.quantum-machines.co/products/opx/.
[51]IBM, Goldeneye cryogenic concept system, 2022, https://research.ibm.com/blog/goldeneye-cryogenic-concept-system.
[52]S. Chen, "Are quantum computers really energy efficient?," Nat. Comput. Sci. **3**(6), 457–460 (2023).
[53]M. Fellous-Asiani, J. H. Chai, Y. Thonnart, H. K. Ng, R. S. Whitney, and A. Auffèves, "Optimizing resource efficiencies for scalable full-stack quantum computers," PRX Quantum **4**(4), 040319 (2023).
[54]T. Walter, P. Kurpiers, S. Gasparinetti, P. Magnard, A. Potočnik, Y. Salathé, M. Pechal, M. Mondal, M. Oppliger, C. Eichler, and A. Wallraff, "Rapid high-fidelity single-shot dispersive readout of superconducting qubits," Phys. Rev. Appl. **7**(5), 054020 (2017).
[55]D. P. DiVincenzo, "Fault-tolerant architectures for superconducting qubits," Phys. Scr. **T137**, 014020 (2009).
[56]R. Barends, J. Kelly, A. Megrant, A. Veitia, D. Sank, E. Jeffrey, T. C. White, J. Mutus, A. G. Fowler, B. Campbell, Y. Chen, Z. Chen, B. Chiaro, A. Dunsworth, C. Neill, P. O'Malley, P. Roushan, A. Vainsencher, J. Wenner, A. N. Korotkov, A. N. Cleland, and J. M. Martinis, "Superconducting quantum circuits at the surface code threshold for fault tolerance," Nature **508**(7497), 500–503 (2014).
[57]E. Charbon, F. Sebastiano, A. Vladimirescu, H. Homulle, S. Visser, L. Song, and R. M. Incandela, "Cryo-cmos for quantum computing," in *2016 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2016), pp. 13–511354.
[58]F. Sebastiano, J. P. G. Van Dijk, P. A. Thart, B. Patra, J. Van Staveren, X. Xue, C. G. Almudever, G. Scappucci, M. Veldhorst, L. M. K. Vandersypen, A. Vladimirescu, S. Pellerano, M. Babaie, and E. Charbon, "Cryo-CMOS interfaces for large-scale quantum computers," in *Technical Digest - International Electron Devices Meeting, IEDM, Vol. 2020-December* (Institute of Electrical and Electronics Engineers, Inc., 2020), pp. 1–25.
[59]F. Sebastiano, H. Homulle, B. Patra, R. Incandela, J. Van Dijk, L. Song, M. Babaie, A. Vladimirescu, and E. Charbon, "Cryo-CMOS electronic control for scalable quantum computing: Invited," in *Proceedings - Design Automation Conference, Vol. Part 128280* (Institute of Electrical and Electronics Engineers, Inc., 2017).
[60]B. Patra, R. M. Incandela, J. P. G. Van Dijk, H. A. R. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastiano, and E. Charbon, "Cryo-CMOS circuits and systems for quantum computing applications," IEEE J. Solid-State Circuits **53**(1), 309–321 (2018).
[61]F. Imroze, F. Nikbakhtnasrabadi, S. Danilin, A. Muhammad, M. Ahmad, C. Giagkoulovits, H. Heidari, and M. Weides, "Packaged CMOS cryogenic characterization for quantum computing applications," in *ICECS 2022 - 29th IEEE International Conference on Electronics, Circuits and Systems, Proceedings* (Institute of Electrical and Electronics Engineers, Inc., 2022).
[62]C. Giagkoulovits, M. Ahmad, F. Nikbakhtnasrabadi, F. Imroze, M. Weides, and H. Heidari, "CryoCMOS characterization strategies and challenges," in *ICECS 2022-29th IEEE International Conference on Electronics, Circuits and Systems, Proceedings* (Institute of Electrical and Electronics Engineers, Inc., 2022).
[63]J. C. Bardin, T. White, M. Giustina, K. J. Satzinger, K. Arya, P. Roushan, B. Chiaro, J. Kelly, Z. Chen, B. Burkett, Y. Chen, E. Jeffrey, A. Dunsworth, A. Fowler, B. Foxen, C. Gidney, R. Graff, P. Klimov, J. Mutus, M. J. McEwen, M. Neeley, C. J. Neill, E. Lucero, C. Quintana, A. Vainsencher, H. Neven, J. Martinis, T. Huang, S. Das, D. T. Sank, O. Naaman, A. E. Megrant, and R. Barends, "Design and characterization of a 28-nm Bulk-CMOS cryogenic quantum controller dissipating less than 2 mW at 3 K," IEEE J. Solid-State Circuits **54**(11), 3043–3060 (2019).
[64]M. Mehrpoo, B. Patra, J. Gong, J. P. G. van Dijk, H. Homulle, G. Kiene, A. Vladimirescu, F. Sebastiano, E. Charbon, and M. Babaie, "Benefits and challenges of designing cryogenic CMOS RF circuits for quantum computers," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)* (IEEE, 2019), pp. 1–5.
[65]E. Charbon, M. Babaie, A. Vladimirescu, and F. Sebastiano, "Cryogenic CMOS circuits and systems: Challenges and opportunities in designing the electronic interface for quantum processors," IEEE Microwave Mag. **22**(1), 60–78 (2021).
[66]S. J. Pauka, K. Das, R. Kalra, A. Moini, Y. Yang, M. Trainer, A. Bousquet, C. Cantaloube, N. Dick, G. C. Gardner, M. J. Manfra, and D. J. Reilly, "A cryogenic CMOS chip for generating control signals for multiple qubits," Nat. Electron. **4**(1), 64–70 (2021).
[67]I. Fiheon, Y. Bhavani, K. Naveen, E. Mostafa, A. Meraj, R. Graham, G. Vihar, H. Hadi, and M. Weides, Adv. Intell. Syst. (published online 2025).
[68]F. Imroze, B. Yalagala, M. Ahmad, M. Elsayed, R. Graham, G. Colletta, H. Heidari, and M. Weides, "Hysteresis-induced neuromorphic behavior in 180nm bulk PMOS devices at 3K," in *2025 IEEE 37th International Conference on Microelectronic Test Structures (ICMTS)* (IEEE, 2025), pp. 1–4.
[69]Y. Zhang, J. Xu, T. T. Lu, Y. Zhang, C. Luo, and G. Guo, "Hot carrier degradation in MOSFETs at cryogenic temperatures down to 4.2 K," IEEE Trans. Device Mater. Reliab. **21**(4), 620–626 (2021).
[70]A. Beckers, F. Jazaeri, and C. Enz, "Characterization and modeling of 28-nm bulk CMOS technology down to 4.2 K," IEEE J. Electron Devices Soc. **6**, 1007–1018 (2018).
[71]T. T. Lu, Z. Li, C. Luo, J. Xu, W. Kong, and G. Guo, "Characterization and modeling of 0.18 μm bulk CMOS technology at sub-kelvin temperature," IEEE J. Electron Devices Soc. **8**, 897–904 (2020).
[72]F. Imroze, N. Kumar, F. Adamu-Lema, V. Georgiev, H. Heidari, and M. Weides, "Linear variation of threshold voltage with back bias for 22nm FDSOI at cryogenic temperature," in *2025 Device Research Conference (DRC)* (IEEE, 2025), pp. 1–2.
[73]L. Le Guevel, G. Billiot, B. Cardoso Paz, M. L. V. Tagliaferri, S. De Franceschi, R. Maurand, M. Cassé, M. Zurita, M. Sanquer, M. Vinet, X. Jehl, A. G. M. Jansen, and G. Pillonnet, "Low-power transimpedance amplifier for cryogenic integration with quantum devices," Appl. Phys. Rev. **7**(4), 041407 (2020).
[74]Y. Yang, K. Das, A. Moini, and D. J. Reilly, "A Cryo-CMOS voltage reference in 28 nm FDSOI," IEEE Solid-State Circuits Lett. **3**, 186 (2020).
[75]T. Dutta, F. Imroze, F. Adamu-Lema, H. Heidari, and M. Weides, "Interplay of short-channel and narrow-width effects in FDSOI transistors at cryogenic temperatures," IEEE Trans. Electron Devices **72**(7), 3407–3414 (2025).
[76]J. van Dijk, P. Hart, G. Kiene, R. Overwater, P. Padalia, J. van Staveren, M. Babaie, A. Vladimirescu, E. Charbon, and F. Sebastiano, "Cryo-CMOS for

analog/mixed-signal circuits and systems," in *2020 IEEE Custom Integrated Circuits Conference (CICC)* (IEEE, 2020), pp. 1–8.
[77]J. Yoo, Z. Chen, F. Arute, S. Montazeri, M. Szalay, C. Erickson, E. Jeffrey, R. Fatemi, M. Giustina, M. Ansmann, E. Lucero, J. Kelly, and J. C. Bardin, "34.2 A 28-nm Bulk-CMOS IC for full control of a superconducting quantum processor unit-cell," in *Digest of Technical Papers-IEEE International Solid-State Circuits Conference, Vol. 2023-February* (Institute of Electrical and Electronics Engineers, Inc., 2023), pp. 506–508.
[78]J. Park, S. Subramanian, L. Lampert, T. Mladenov, I. Klotchkov, D. J. Kurian, E. Juarez-Hernandez, B. P. Esparza, S. R. Kale, K. T. Asma Beevi, S. P. Premaratne, T. F. Watson, S. Suzuki, M. Rahman, J. B. Timbadiya, S. Soni, and S. Pellerano, "A fully integrated Cryo-CMOS SoC for state manipulation, readout, and high-speed gate pulsing of spin qubits," IEEE J. Solid-State Circuits **56**(11), 3289–3306 (2021).
[79]S. Chakraborty, D. J. Frank, K. Tien, P. Rosno, M. Yeck, J. A. Glick, R. Robertazzi, R. Richetta, J. F. Bulzacchelli, D. Underwood, D. Ramirez, D. Yilma, A. Davies, R. V. Joshi, S. D. Chambers, S. Lekuch, K. Inoue, D. Wisnieff, C. W. Baks, D. S. Bethune, J. Timmerwilke, T. Fox, P. Song, B. R. Johnson, B. P. Gaucher, and D. J. Friedman, "A Cryo-CMOS low-power semi-autonomous transmon qubit state controller in 14-nm FinFET technology," IEEE J. Solid-State Circuits **57**(11), 3258–3273 (2022).
[80]European Union, European chips joint undertaking: ARCTIC, 2024, https://arctic-kdt.eu/.
[81]E. Leonard, M. A. Beck, J. Nelson, B. G. Christensen, T. Thorbeck, C. Howington, A. Opremcak, I. V. Pechenezhskiy, K. Dodge, N. P. Dupuis, M. D. Hutchings, J. Ku, F. Schlenker, J. Suttle, C. Wilen, S. Zhu, M. G. Vavilov, B. L. T. Plourde, and R. McDermott, "Digital coherent control of a superconducting qubit," Phys. Rev. Appl. **11**(1), 014009 (2019).
[82]C. H. Liu, A. Ballard, D. Olaya, D. R. Schmidt, J. Biesecker, T. Lucas, J. Ullom, S. Patel, O. Rafferty, A. Opremcak, K. Dodge, V. Iaia, T. McBroom, J. L. Dubois, P. F. Hopkins, S. P. Benz, B. L. T. Plourde, and R. McDermott, "Single flux quantum-based digital control of superconducting qubits in a multichip module," PRX Quantum **4**(3), 030310 (2023).
[83]K. Likharev and V. Semenov, "RSFQ Logic/memory family: A new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," IEEE Trans. Appl. Supercond. **1**(1), 3 (1991).
[84]P. Bunyk, K. Likharev, and D. Zinoviev, "RSFQ technology: Physics and devices," Int. J. High Speed Electron. Syst. **11**(1), 257–305 (2001).
[85]W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, "Rapid single flux quantum T-Flip flop operating up to 770 GHz," Technical Report No. 2, 1999.
[86]J. Barbosa, J. C. Brennan, A. Casaburi, M. D. Hutchings, A. Kirichenko, O. Mukhanov, and M. Weides, "RSFQ all-digital programmable multi-tone generator for quantum applications," IEEE Trans. Quantum Eng. **6**, 5500211 (2025).
[87]R. McDermott and M. G. Vavilov, "Accurate qubit control with single flux quantum pulses," Phys. Rev. Appl. **2**(1), 014007 (2014).
[88]X. Geng, K. He, R. Huang, J. Liu, W. Chen, L. Yang, X. Wu, Q. Yu, M. Cheng, G. Chen, J. Liu, and W. Chen, "Qubit energy tuner based on single flux quantum circuits," Front. Phys. **11**, 1215468 (2023).
[89]K. Li, R. McDermott, and M. G. Vavilov, "Hardware-efficient qubit control with single-flux-quantum pulse sequences," Phys. Rev. Appl. **12**(1), 014044 (2019).
[90]M. R. Jokar, R. Rines, and F. T. Chong, "Practical implications of SFQ-based two-qubit gates," in *Proceedings - 2021 IEEE International Conference on Quantum Computing and Engineering, QCE 2021* (Institute of Electrical and Electronics Engineers, Inc, 2021), pp. 402–412.
[91]J. Bernhardt, C. Jordan, J. Rahamim, A. Kirchenko, K. Bharadwaj, L. Fry-Bouriaux, K. Porsch, A. Somoroff, K.-T. Tsai, J. Walter, A. Weis, M.-J. Yu, M. Renzullo, D. Yohannes, I. Vernik, O. Mukhanov, and S. J. Han, "Quantum computer controlled by superconducting digital electronics at millikelvin temperature," arXiv:2503.09879 (2025).
[92]A. Opremcak, I. V. Pechenezhskiy, C. Howington, B. G. Christensen, M. A. Beck, E. Leonard, J. Suttle, C. Wilen, K. N. Nesterov, G. J. Ribeill, T. Thorbeck, F. Schlenker, M. G. Vavilov, B. L. T. Plourde, and R. McDermott, "Measurement of a superconducting qubit with a microwave photon counter," Science **361**(6408), 1239–1242 (2018).
[93]C. Howington, A. Opremcak, R. McDermott, A. Kirichenko, O. A. Mukhanov, and B. L. T. Plourde, "Interfacing superconducting qubits with cryogenic logic: Readout," IEEE Trans. Appl. Supercond. **29**(5), 1700305 (2019).
[94]L. Di Palma, A. Miano, P. Mastrovito, D. Massarotti, M. Arzeo, G. P. Pepe, F. Tafuri, and O. Mukhanov, "Discriminating the phase of a coherent tone with a flux-switchable superconducting circuit," Phys. Rev. Appl. **19**(6), 064025 (2023).
[95]L. Howe, M. Castellanos-Beltran, A. J. Sirois, D. Olaya, J. Biesecker, P. D. Dresselhaus, S. P. Benz, and P. F. Hopkins, "Digital control of a superconducting qubit using a Josephson pulse generator at 3 K," PRX Quantum **3**(1), 010350 (2022).
[96]R. McDermott, M. G. Vavilov, B. L. T. Plourde, F. K. Wilhelm, P. J. Liebermann, O. A. Mukhanov, and T. A. Ohki, "Quantum-classical interface based on single flux quantum digital logic," Quantum Sci. Technol. **3**(2), 024004 (2018).
[97]N. Takeuchi, T. Yamae, T. Yamashita, T. Yamamoto, and N. Yoshikawa, "Microwave-multiplexed qubit controller using adiabatic superconductor logic," npj Quantum Inf. **10**(1), 53 (2024).
[98]A. Youssefi, I. Shomroni, Y. J. Joshi, N. R. Bernier, A. Lukashchuk, P. Uhrich, L. Qiu, and T. J. Kippenberg, "A cryogenic electro-optic interconnect for superconducting devices," Nat. Electron. **4**(5), 326–332 (2021).
[99]F. Lecocq, F. Quinlan, K. Cicak, J. Aumentado, S. A. Diddams, and J. D. Teufel, "Control and readout of a superconducting qubit using a photonic link," Nature **591**(7851), 575–579 (2021).
[100]G. Sinatkas, T. Christopoulos, O. Tsilipakos, and E. E. Kriezis, *Electro-Optic Modulation in Integrated Photonics* (American Institute of Physics, Inc., 2021).
[101]P. O. Weigel, J. Zhao, K. Fang, H. Al-Rubaye, D. Trotter, D. Hood, J. Mudrick, C. Dallo, A. T. Pomerene, A. L. Starbuck, C. T. DeRose, A. L. Lentine, G. Rebeiz, and S. Mookherjea, "Bonded thin film lithium niobate modulator on a silicon photonics platform exceeding 100 GHz 3-dB electrical modulation bandwidth," Opt. Express **26**(18), 23728 (2018).
[102]K. Yoshida, Y. Kanda, and S. Kohjiro, "A traveling-wave-type $LiNbO_3$ optical modulator with superconducting electrodes," Technical Report No. 7, 1999.
[103]M. de Cea, E. E. Wollman, A. H. Atabaki, D. J. Gray, M. D. Shaw, and R. J. Ram, "Photonic readout of superconducting nanowire single photon counting detectors," Sci. Rep. **10**(1), 9470 (2020).
[104]F. Thiele, T. Hummel, A. N. McCaughan, J. Brockmeier, M. Protte, V. Quiring, S. Lengeling, C. Eigner, C. Silberhorn, and T. J. Bartley, "All optical operation of a superconducting photonic interface," Opt. Express **31**, 32717 (2023).
[105]G. Arnold, T. Werner, R. Sahu, L. N. Kapoor, L. Qiu, and J. M. Fink, "All-optical superconducting qubit readout," Nat. Phys. **21**, 393–400 (2025).
[106]A. Al-Moathin, M. Zhong, Q. Al-Taai, Y. Jiang, M. Farage, J. U. R. Kazim, M. Z. Ali, F. Nikbakhtnasrabadi, M. Powell, P. Khatri, M. Stanley, A. Rossi, H. Heidari, M. A. Imran, Q. H. Abbasi, N. M. Ridler, M. Weides, and C. Li, "Characterization of a compact wideband microwave metasurface lens for cryogenic applications," in *2023 101st ARFTG Microwave Measurement Conference* (IEEE, 2023), pp. 1–4.
[107]J. u. Rehman Kazim, M. Z. Ali, A. Al-Moathin, F. Nikbakhtnasrabadi, P. Khatri, M. Powell, M. Stanley, N. M. Ridler, A. Rossi, M. Weides, H. Heidari, M. A. Imran, Q. H. Abbasi, and C. Li, "Wireless microwave signal transmission for cryogenic applications," in *2023 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting* (IEEE, 2023), pp. 43–44.
[108]J. Wang, M. I. Ibrahim, I. B. Harris, N. M. Monroe, M. I. Wasiq Khan, X. Yi, D. R. Englund, and R. Han, "34.1 THz Cryo-CMOS backscatter transceiver: A contactless 4 Kelvin-300 Kelvin data interface," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference, Vol. 2023-February* (Institute of Electrical and Electronics Engineers, Inc, 2023), pp. 504–506.
[109]J. Anders, M. Babaie, J. C. Bardin, I. Bashir, G. Billiot, E. Blokhina, S. Bonen, E. Charbon, J. Chiaverini, I. L. Chuang, C. Degenhardt, D. Englund, L. Geck, L. Le Guevel, D. Ham, R. Han, M. I. Ibrahim, D. Krüger, K. M. Lei, A. Morel *et al.*, "CMOS integrated circuits for the quantum information sciences," IEEE Trans. Quantum Eng. **4**, 5100230 (2023).
[110]E. Alarcon, S. Abadal, F. Sebastiano, M. Babaie, E. Charbon, P. H. Bolivar, M. Palesi, E. Blokhina, D. Leipold, B. Staszewski, A. Garcia-Saez, and C. G. Almudever, "Scalable multi-chip quantum architectures enabled by cryogenic hybrid wireless/quantum-coherent network-in-package," in *Proceedings - IEEE International Symposium on Circuits and Systems, Vol. 2023-May* (Institute of Electrical and Electronics Engineers, Inc., 2023).
[111]A. Anferov, F. Wan, S. P. Harvey, J. Simon, and D. I. Schuster, "Millimeter-wave superconducting qubit," PRX Quantum **6**, 020336 (2025).

[112]J. Wang, I. Harris, M. Ibrahim, D. Englund, and R. Han, "A wireless terahertz cryogenic interconnect that minimizes heat-to-information transfer," Nat. Electron. **8**, 426 (2025).
[113]M. Shen, J. Xie, Y. Xu, S. Wang, R. Cheng, W. Fu, Y. Zhou, and H. X. Tang, "Photonic link from single-flux-quantum circuits to room temperature," Nat. Photonics **18**(4), 371–378 (2024).
[114]R. Acharya, S. Brebels, A. Grill, J. Verjauw, T. Ivanov, D. P. Lozano, D. Wan, J. Van Damme, A. M. Vadiraj, M. Mongillo, B. Govoreanu, J. Craninckx, I. P. Radu, K. De Greve, G. Gielen, F. Catthoor, and A. Potočnik, "Multiplexed superconducting qubit control at millikelvin temperatures with a low-power cryo-CMOS multiplexer," Nat. Electron. **6**, 900–909 (2023).
[115]M. Jerger, S. Poletto, P. Macha, U. Hübner, E. Il'ichev, and A. V. Ustinov, "Frequency division multiplexing readout and simultaneous manipulation of an array of flux qubits," Appl. Phys. Lett. **101**(4), 042604 (2012).
[116]IBM Quantum: The IBM Quantum Roadmap, 2024, https://www.ibm.com/quantum/blog/ibm-quantum-roadmap (accessed 05 November 2024).