

**Surface Insulation
Resistance Measurements:
A Review of the
Various SIR Parameters**

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Surface Insulation Resistance Measurements
A Review of the Significance and Sensitivity of
the Various SIR Parameters

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ABSTRACT

As part of a larger study of the cleanliness and reliability of soldered joints a study of the significance and sensitivity of the various SIR parameters is discussed and recommendations for the future of SIR testing made. A full consideration of the many parameters has led to an improved methodology which permits a more meaningful test to be conducted. It is clear from recent developments that the standards making organisations are now incorporating many of the ideas developed in this report.

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Approved on behalf of Managing Director, NPL,
by Dr M K Hossain, Director, Centre of Materials Measurement and Technology

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1 INTRODUCTION

The cleaning of PCBs after the soldering of components is normally carried out to remove contaminant materials (such as flux residues) that might compromise the service life if left on the PCB and to provide a clean surface for good adhesion of any conformal coatings subsequently applied. In order to ensure an adequate level of cleanliness has been achieved the effectiveness of the cleaning process is monitored using one of two basic types of test:

- 1 A cleanliness monitor to assess the actual levels of soils on the PCBs; these results can be available in under an hour.
- 2 An accelerated test to assess the effects that the soils have on the reliability of the PCB; these results may take days or weeks to obtain.

The first method employs solvent extract conductivity (SEC) techniques using a mixture of alcohol and water (1). These techniques rely on dissolving the soils in alcohol (usually isopropanol), while at the same time taking any ionic species into the water. A conductivity meter is then used to monitor the change in the fluid resistance and thereby the amount of ionic material removed. This is used as a measure of the amount of soil on the PCB being assessed. This technique has the disadvantage that modern organic acid based fluxes do not always result in an increase in the conductivity of the extract solution.

In the second method (1) a test pattern usually composed of interdigitated metal fingers on the surface of the PCB is exposed to an accelerating test environment of temperature and humidity under bias. Any effect that the soils have on the surface insulation resistance of the PCB is monitored.

A study of the issues involved is presented here to provide recommendations for the philosophy and measurement rationale of SIR.

The issues addressed were:-

- a Review of current and potential SIR Procedures
- b Analysis of the significance and sensitivity of SIR parameters
- c Recommendations for the future

The review of the first item, the current SIR procedures, has already been reported (2a) and it is the purpose of this report to address the last two of these items.

2 CURRENT TEST PROCEDURES

There is a plethora of SIR test methods that can be applied (3) at any number of different stages

of the production of a PCB (e.g. IPC-TM-650, Method 2.5.27, "Surface Insulation Resistance of Raw, Printed Wiring Board Material" to IPC-TM-650, Method 2.6.3.3, "Moisture and Surface Insulation Resistance, Fluxes"). Each method is designed to evaluate a particular aspect of the reliability of the PCB, such as the basic raw material, the conformal coating or the flux used during assembly. As already mentioned a review of those test regimes that can be applied to "completed" assemblies has already been reported (2a). However since that report was issued a number of changes have occurred in this field (4,5) and these are reported in the following two Sections.

2.1 IPC-TM-650 Method 2.6.3.3 (Moisture and Surface Insulation Resistance, Fluxes)

The parameters used in this method have been reassessed and revised, and both revision 2.6.3.3 and the newer 2.6.3.3 Revision A, will be discussed below. The method attempts to define the majority of the parameters of the test, such as the pre-preparation of the sample, test voltages, conditions and duration. However, unlike the Bellcore test the decision with respect to pass/fail criteria is still left to the user/customer.

Pattern Style.

The original specification called for the use of one of the comb patterns from the IPC-B-25 test pattern. Each consists of a series of interdigitated lines with spacings of either 0.025", 0.0125" or 0.0065". Each pattern is divided into five sections, three on one side of the comb and two on the other with staggered overlap (see Figure 1). The actual pattern specified in this particular test is that with the 0.0125" line spacing.

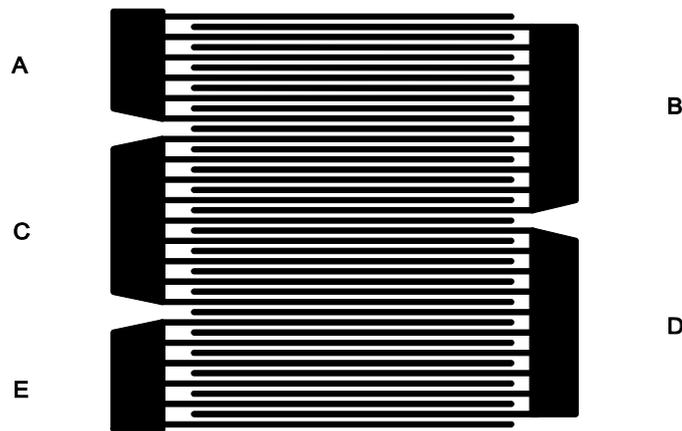


Figure 1. A schematic representation of the layout of an IPC-B-25 SIR test pattern using a line width and track spacing of 0.0125".

The latest revision of the test method incorporates a change in the test pattern from the segmented design shown above to a straightforward set of interdigitated fingers with only a single contact on each side as detailed in IPC-B-24. The basic pattern, of which there are four per test coupon, is shown in Figure 2 below.

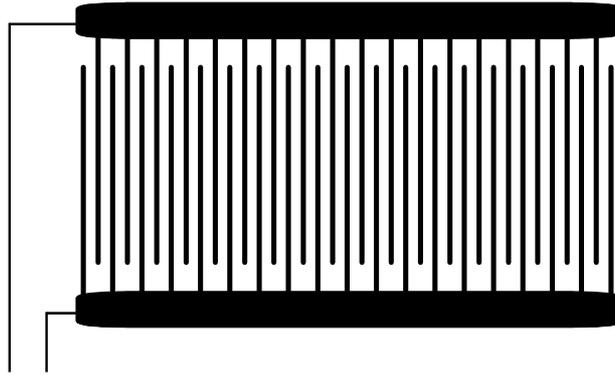


Figure 2. Schematic of IPC-B-24 SIR test pattern (spacing; line 0.4mm; track 0.5mm).

Sample Population

In common with the majority of its counterparts the original test specification did not give any indication as to the number of samples that should be tested, the choice being left to the discretion of the user. In the latest specification the user is required to carry out a matrix test involving the use of at least two ".....unprocessed control coupons for comparison purposes" and a variable number of actual test coupons depending upon whether the user is evaluating a liquid flux (for wave soldering applications) or a solder paste (for solder paste applications).

Environmental Test Conditions

The original method defined three sets of test conditions for use. The first two appeared to be identical, and are identified as Class 1 (consumer applications) and Class 2 (industrial applications). They required that the boards under test be subjected to an environment of $50\pm 2^{\circ}\text{C}/90\%$ relative humidity for a minimum of 168 hours. The third, Class 3 (military and high reliability electronics) required the test conditions to be $85\pm 2^{\circ}\text{C}/85\%$ relative humidity also for a minimum of 168 hours. The latest test specification requires only a single condition of $85\pm 2^{\circ}\text{C}$, $85\pm 2\%$ relative humidity for 168 hours.

Electrical Test Conditions

In all three classes of the original test method the patterns were required to be biased at 45-50 V(DC) throughout the environmental exposure. The bias voltage is applied in such a way that the contacts A, C and E are positive, and B and D are negative. Prior to measurements of the insulation resistance the bias voltage is raised to 100 V(DC) and the polarity is reversed and held for one minute. The actual measurements are made between the various segments into which each pattern is divided thus enabling, in theory, individual assessment of the performance across the various parts of the test pattern. That is, measurements were to be made across A to B, B to C, C to D and D to E, at intervals of 24, 96 and 168 hours within the test chamber. At no time were the boards to be allowed to cool or dry until after the final electrical measurements had been made.

The latest revision still uses a bias voltage of 45-50V and a measurement voltage of -100V, and still leaves the ultimate pass/fail criteria to the user/customer. However, an additional parameter has been added in the form of a requirement that the values obtained from the control

coupons should at no time be less than 1000 MΩ. If such a value is obtained then the whole test must be repeated.

Evaluation of Results

Although readings of the surface insulation resistance are taken at several points in time, only those made after 96 or 168 hours are used to classify the flux performance. The determination of a pass/fail criterion is left to the user/customer.

2.2 ISO Test Specification (Proposed)

This proposed test specification (5) seeks to define the conditions required to determine the extent of any deleterious effects via an assessment of the surface insulation resistance resulting from the presence of flux residues after soldering. All stages of a surface insulation resistance test from the test pattern to be used, through the bias conditions, to evaluation of the results with respect to a pass/fail criterion, are defined.

Pattern Style.

The pattern in this proposed specification is defined as ".....conforming to IPC-B-25 Pattern B as detailed in IPC-TM-650." However, unlike the IPC-B-25 pattern (Figure 1) the proposed ISO pattern is not divided into five separate sections that are interleaved, but consists of two interleaved combs as shown below in Figure 3.

Sample Population

This particular test method requires a minimum of seven test samples each of which contains four test patterns. The total number of the samples depends upon whether a liquid flux or solder paste is under test, but in either case a single control sample is retained.

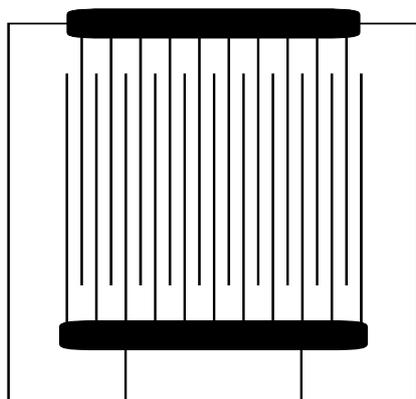


Figure 3. Schematic of the layout of the proposed ISO test specification.

Environmental Test Conditions

The test method requires the samples to be exposed to an environment of either 40°C/95% relative humidity or 85°C/85% relative humidity for a total time of 264 hours.

Electrical Test Conditions

The conditions of this test are the same as those of the IPC-TM-650 test method, i.e. the patterns are biased at 45-50 V(DC) throughout the environmental exposure, with a reversed -100 V(DC) bias applied for one minute prior to the measurement of the surface insulation resistance.

Evaluation of Results

Although the method states that all the test boards and patterns should achieve a minimum insulation resistance of $10^{12}\Omega$ after preconditioning but prior to the application of the flux, and that the control board SIR values after environmental testing should not have altered by more than a factor of ten for the whole test to be considered valid, no indication is given as to what constitutes a pass/fail limit. In addition, the proposed specification requires that the results of the electrical measurements made after preconditioning, and after four and eleven days of total exposure to the environmental testing, be recorded. There is as yet no indication as to what should be considered good or bad performance.

3 AN ANALYSIS OF THE SIGNIFICANCE AND SENSITIVITY OF PARAMETERS

There are many factors that affect the value of the surface insulation resistance measured during a test. These factors range from those resulting from the actual materials from which the PCB is made, the fabrication process itself, to the manner in which the test samples were prepared and tested. *Since current specifications do little to explain how the actual SIR test is carried out, it is necessary to develop and document a detailed procedure. Moreover, valid SIR tests and results require careful planning from inception, choice of parameters and materials, testing, to data collection and analysis.* In consequence, the following Sections discuss a number of the relevant issues.

3.1 The Test Board

The design and construction of the test board are just as important as the test method. Indeed, there are a number of parameters within the simple heading of test board that must be considered when determining the most effective and realistic SIR test to be carried out.

3.1.1 Test Board Material

The most commonly encountered substrate material in microelectronics is the FR4 (glass fibre reinforced resin) PCB. It is this material that forms the bulk of most products that are available and around which nearly all SIR tests are based. Alternatives are available (e.g. FR2 or alumina)

but are less commonly encountered or specified for actual use except in instances, say, of especially low cost (FR2) or high value/reliability (alumina). Although the test method is referred to as a surface insulation resistance test the effects that the bulk material may have on the results obtained cannot be ignored and certain steps must be taken to minimise them.

In the case of a poorly manufactured FR4 test board, ionic species may be able to migrate from, or be leached from, the bulk to the surface throughout the SIR test, producing anomalously low SIR values. These species may be present as a result of a number of factors such as incomplete cure of the resin, poor mixing of the original components, or constituent materials beyond their shelf life. None of these would be expected to occur often, and not at all within a well run assembly facility. But experience has shown (2b) that it is often wise (and can save much time and energy in invalid testing) to investigate (using FTIR or Differential Scanning Calorimetry for example) a small sample of incoming boards for incomplete curing etc, or even subject a few as-delivered boards to a "dummy" SIR test.

Another factor to be considered is the surface finish of the substrates. FR4 boards often contain surface asperities that can trap ionic residues and retain them through subsequent processing stages. During the longer times of the SIR test (tens of hours) as opposed to the comparatively short cleaning times (tens of minutes) those residues can migrate to the surface of the board. This is a well recognised problem (2b) and in general the solution adopted is to ensure good quality control of all feedstock, and thorough cleaning immediately prior to the application of the solder resist layer, the final stage of the substrate fabrication before components are added. In contrast, alumina substrates generally have very few surface pores to trap and retain ionic species from the preparation stages, suggesting that it would be preferable to use an alumina test substrate during testing. However, the aim of the testing is to assess the actual service performance of the product and the use of an alumina test substrate to evaluate a process that is based around an FR4 substrate is unrealistic.

Summary: *For reliable SIR testing it is necessary to ensure a good and consistent quality of test substrates (re materials and fabrication).*

3.1.2 Electrode Material

Once the test substrate has been selected the electrode material must be chosen. In general this is a simple task based upon the type of substrate in use. If the test board is based on FR4 then the electrode material will be copper, which may or may not be (6) coated in a layer of tin. In such circumstances there are two basic methods of patterning the substrate; one is to cover the whole surface with the copper and then etch away the unrequired regions, the other is to apply the copper only where it is required. In either case the final patterned substrate will be heavily contaminated with ionic species that would adversely affect the subsequent processing (e.g. adhesion of solder resist) and the SIR performance. Therefore common practice demands a good cleaning process to remove these contaminants.

Other electrode materials sometimes used are gold and silver-palladium. However, these are usually confined to alumina substrates for high reliability applications and will not be considered further. In all cases the pattern should be visually inspected to ensure it conforms precisely to that specified, and does not contain etching defects. If such etching defects do exist they can lead to anomalous SIR results (2b).

Summary: *For reliable SIR testing it is necessary to ensure that test boards, whether tinned or not, are thoroughly cleaned to remove all ionic contamination.*

3.1.3 Pattern Design

Unfortunately, there exists an ever increasing number of designs of SIR test pattern (4,5,7,8) both within the existing national standards and within specifications and designs developed (9) for specific purposes. All these patterns have certain aspects in common and differ generally only in scope and application. However, it should be emphasised that SIR tests using different patterns will yield different resistance values even when the contamination levels are the same.

Track Spacing

The track spacing of the test pattern should be representative of the product being evaluated. A successful SIR test on a pattern with a large gap cannot be taken as evidence that PCBs assembled with a smaller track spacing would give good field and life performance. The size of the spacing (in combination with the applied test voltage) determines the field across the gap and this must not exceed the dielectric breakdown strength of the substrate material. A commonly used test pattern (A, IPC-B-25) has spacings of 0.165mm, and 100V applied across this spacing gives a voltage gradient of ~600V/mm, which is more than five times the maximum advocated by MIL-STD-275 for circuits functioning under normal conditions (10). The use of lower test voltages should therefore be given every consideration. The voltage drop is clearly the driving force for the migration of ionic species and possibly dendritic growth. While the user/customer may wish to maximize this voltage drop in order to reduce the test time, care must be taken not to create a situation of abuse rather than accelerated testing.

Pattern Geometry

If the pattern incorporates sharp corners then current crowding will occur at these points. The result will be an artificially high field. This is not desirable. Obviously the acceptance of design guidelines that eliminate this possibility is good practice, and requires only that the tips and corners of the SIR test pattern be rounded.

Guard Banding

Since a test board can contain a number of discrete SIR patterns, the connecting tracks of which will be brought out to a single edge, there is clearly the danger that leakage could occur between one pattern and another. The current flowing as a result of such leakage would clearly be indistinguishable from (and additive to) the intrinsic current resulting from any soils present. Since SIR currents are usually measured at the earthy end of the circuit it is a simple matter to ensure that no additional current is detected by the use of guard banding in which each pattern and each output lead is surrounded by a grounded track (2a).

Pattern Style and Placement

Traditionally SIR test patterns have involved the use of two interdigitated combs (see Figures 1 to 3) that are oppositely biased, and any changes in resistance between the two halves of the pattern is monitored as evidence of change caused by the presence of contaminants. This type of pattern was conceived when the common forms of assembly involved the use of wave soldering followed by a cleaning stage that ensured that the whole surface of the board was covered first in flux and then in "uncontaminated" cleaning fluid. The result was that if any contamination were present, the surface of the PCB could be reasonably assumed to be uniformly "contaminated". Such wave soldering processes are still employed and the use of these patterns is still perfectly valid. However, other options must be considered, in particular when evaluating the reliability of a PCB incorporating surface mount devices which are attached by reflowing screen printed solder paste in small discrete areas.

It is generally accepted that the most difficult components to clean under are large surface mount packages (9) with either low stand-off heights (e.g. Quad Flat Packs), restricted access to

the area beneath the component (e.g. Ball Grid Arrays), or both (e.g. Leadless Ceramic Chip Carriers). Hence a test method not involving the use of such component-board combinations cannot be used to evaluate an assembly process that is designed for populated boards. Most cleaning regimes incorporate a series of stages each of which is progressively cleaner than the preceding one. When a PCB has been assembled and soldered it is effectively dry, thus when it is subjected to the first cleaning stage there will be good wetting beneath the components. However, solvent quickly becomes dirty (leading to poor wetting) and must be replaced in the subsequent cleaning stages. The rate at which this happens will be determined by (i) the access available, and (ii) whether assisted cleaning is available e.g. via ultrasonic agitation, submerged directed jetting, high pressure sprays, or vigorous agitation. It is therefore sensible to provide for the placement of a demanding component over a SIR test pattern to replicate the problems of cleaning an area of restricted access.

Another trend within the electronics industry is towards the use of reflow soldering (often infrared, especially in Europe) with no-clean flux technology, i.e. no cleaning after the components have been soldered to the PCB. Any soil left behind by the assembly process is neither removed nor subsequently distributed over the whole surface of the PCB as would happen during cleaning. However, it is concentrated around the package pins, the worst possible location. A standard comb pattern, wherever it was placed on a PCB (either test coupon or actual product) would not be useful in detecting this type of contamination; it

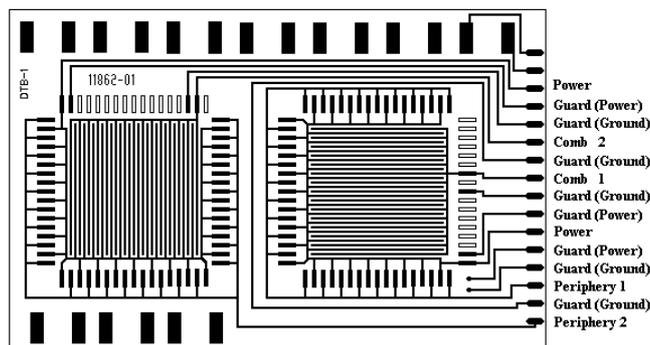


Figure 4. Schematic of test coupon incorporating a combination of a standard and peripheral style comb test patterns.

would simply be in the wrong position. This situation requires a different pattern such as that illustrated in Figure 4. The pads to which the package pins are soldered, are linked alternately, producing a comb pattern around the periphery of the device. This approach can only be used with test devices with no internal connections; any internal electronics would adversely affect the SIR readings obtained.

Summary: *For meaningful SIR testing, standard SIR test patterns appropriate to the test method, should be chosen. If possible, and certainly if the pattern is being specifically generated, it is necessary to ensure the use of realistic field gradients, guard banding, and the ability to assess both populated areas of the board and under demanding components.*

3.1.4 Solder Resist

Once the test substrate and electrode material have been chosen there remains the consideration of whether a solder resist should be applied, and if so, which should be used. If the user/customer is attempting to evaluate a production process which employs a solder resist then a solder resist should be used in the test. Moreover, in order to ensure that a number of manufacturing factors will then remain constant, the solder resist should be that which is used in normal production, being applied in the same manner.

If the underlying substrate has not been adequately cleaned, then the resist may trap any contaminants and prevent their removal during the final cleaning stages of the whole assembly. They can be released, however, during the much longer SIR testing, producing a reduction in the SIR values obtained (2b). This assumes, of course, that the levels of contaminants were not sufficiently high to prevent the resist from adhering to the substrate surface in the first place.

Solder resists also have to be cured. The act of curing increases the extent of the cross-linking of the polymeric structures. This may be achieved by either a thermal bake, an ultraviolet cure, or both. Whatever the method an incomplete cure will result in a poor performance, with possibly the presence of ionic contamination producing poor SIR values (see Section 3.1.1). In general a fully cross-linked structure achieved by the use of an extended thermal bake or UV exposure will result in higher SIR values.

Summary: *For sensible SIR testing the same solder resist should be used as the product under evaluation; it is again essential to ensure proper and consistent processing.*

3.1.5 Conformal Coating

If the final product is to be conformally coated then consideration should be given to the use of such a material during any testing/evaluation. Not only could the application of such a layer add possible contaminants of its own (although obviously all are formulated to minimise this possibility), but if applied incorrectly, the coating may also trap any contaminants on the surface of the PCB.

Summary: *If the final product is to be conformally coated, test samples should be conformally coated using production coatings and production application methods.*

3.1.6 Components

The relevance of components when carrying out SIR testing has already been discussed. If the user is trying to evaluate a total assembly process either using test coupons or actual product, then components must be present. These items may not only bring with them their own contaminants (especially if they are used as delivered from the manufacturer) thus altering "the contamination budget", but more importantly they provide the surface for the flux to act upon. Flux is effectively designed to remove the oxide layer from the package pins and to provide a clean surface for the solder. These processes will produce by-products that may affect not only the overall service performance of the PCB but also any SIR values obtained.

None of the current specifications make provision for the use of components even when the test

regime is designed to evaluate the potential reliability of a finished product.

Summary: *For meaningful SIR testing the boards must be populated (at least partially) with components that provide a searching test of the assembly/cleaning process.*

3.2 Sample Preparation

The process of assembling a PCB involves the use of many materials and stages each of which can contribute its own contaminants to the final soil level. In addition, the contaminants left behind after each stage of the assembly process may react with, or be altered by, the subsequent processing stages to produce yet further contaminants. The levels of all these contaminants may also vary adding yet further variability to the ultimate performance during service or testing of the completed PCB assembly.

The exact nature of the sample preparation will depend upon whether the test is being used as a process monitor/evaluation routine or as an absolute test. In the former case it is obviously of paramount importance that the sample preparation be as representative of the process being monitored/evaluated as possible i.e. the substrate, flux, soldering, pre-cleaning etc, should all be those used during normal assembly. No extra stages should be included to produce "super" clean assemblies to ensure that any specified test criteria are achieved. Indeed, there are arguments to support a "nominal worst case" scenario. In this way a true indication of the performance of the whole system can be achieved, although the contribution of any one individual stage cannot be determined.

Where the test is to be used to evaluate a proposed change in the method/materials of PCB assembly (e.g. to assess the performance of a new solder paste against that currently in use) then ideally all other variable factors should be eliminated i.e. the test PCBs and components must be cleaned before use to remove all pre-existing contamination. The latter may be achieved using a cleaning regime specially established for the purpose but which might be uneconomic on a commercial scale. Such a regime might include a water/isopropanol clean. There are many commercial instruments available for this latter step.

Summary: *The sample preparation for SIR testing must be appropriate to that required by the objective of the test, and should represent materials and processes to be used in production.*

3.3 Test Conditions

The aim of any testing is to accelerate the rate of any degradation in the performance of the PCBs under test, and achieve the necessary data in the minimum test time. There are a number of parameters that may be varied to achieve this acceleration; the key ones are discussed below.

Temperature

There are several test temperatures defined in the test methods, and it is accepted that the use of a high temperature during testing gives the maximum acceleration factor (and hence minimum test time). However, there are limits to the temperature which can be used in the test. It must not modify in any way the materials (or their stability) of the assembly under test. In the past there has been some concern that temperatures in excess of 100°C for extended periods may

induce such changes, and all major methods now restrict test temperatures to less than 100°C.

Moreover, recent work (11-13) suggests that certain fluxes (modern organic acid, water soluble fluxes) which have a significant vapour pressure at elevated temperatures, would entirely evaporate during the course of a "high" temperature test. The SIR test results would therefore be anomalous and misleading, and the work suggests that some acceleration tests may not be appropriate for reliability testing of certain low solids, no-clean fluxes. This aspect is discussed further in Section 5. Hence if the SIR test is to be representative of a life test then under these circumstances the test parameters must be chosen to account fully for this situation.

Humidity

The relative humidity in the atmosphere of the test will define the surface concentration of adsorbed moisture and hence can be used to accelerate any degradation mechanism. The conductance per square of the surface layer is defined as the product of the total number of available mobile species per square area and the mobility and the charge carried by each mobile species. Thus the effect of increasing the relative humidity is to increase the mobility of species available for conduction. The dearth of available data for the relationship between surface moisture concentrations and local relative humidity make an assessment of the accelerating effect of increased humidity levels difficult. In some tests the relative humidity is required to be held at 85% whereas in others it is held at 90%. The difference in the acceleration factor between the two regimes is (14) approximately a factor of two.

The manner in which the humidity is measured can also lead to problems. A comparison of the use of capacitive sensors with wet/dry bulb monitors has demonstrated (15) that only the latter should be used. The capacitive method, which led to consistently high results in that work, is always used by the authors (2b).

The only criterion that can be applied in the selection of the humidity level for accelerated testing is the ease with which it can be guaranteed that condensation will not occur during the test, and on this basis the 85% level is preferred.

Bias Voltage

Another possible method of achieving an acceleration in the test and hence minimising the test time, is the bias voltage (or more accurately the field between tracks). In practice, provided the substrate breakdown voltage is not exceeded, the only effect of increasing the voltage bias level is to increase the current to be measured. The overriding consideration is to attempt to measure the insulation resistance under conditions as close as possible to those experienced by the circuit in the field e.g. voltage gradients (16) of up to ~130 V/mm. As pointed out in Section 3.1.3 a modest inter-track spacing of 0.165mm and a bias voltage of 100V will generate a voltage gradient of ~600 V/mm. It is essential that both the test and measurement voltages are kept within design tolerances to prevent "over-voltage" failures and unrelated failure modes.

One such "unrelated" failure mechanism has been described by Turbini (17) in SIR tests on FR4 boards using 100V at 85°C/85% RH for 28 days. She showed that if high voltage gradients are employed in tests using water-soluble fluxes then conductive anodic filaments are formed. The generation of these copper-containing salts along the glass fibres of the epoxy glass within the board is enhanced by polyglycols in the water-soluble fluxes. It should be noted, however, that a major source of polyglycols in modern printed circuit assemblies comes from the water-soluble fusing fluids used to reflow solder-plated boards or in the hot air levelled (HASL) process.

Duration

The length of test will be determined by the objective of the test as much as by the requirements of any test specification. In general the results are required in the minimum possible time, especially if one is evaluating the potential reliability of finished product for which delivery is dependent upon the successful completion of a SIR test. The temptation in such circumstances is to increase the temperature and/or humidity to achieve the maximum acceleration over normal operating conditions and thereby reduce the test time to a minimum. However, the first step is to calculate how long the PCBs must be subjected to the accelerated test conditions in order to replicate the required service life. The exact acceleration factor will be dependent on the acceleration that can be achieved without promoting failure mechanisms unrelated to those associated with processing/cleaning or those seen in the field. This acceleration factor can then be used in conjunction with the required service life, to determine the test duration. Commonly encountered test times are in the region of 1000 hours (~6 weeks) for projected product life times of 20 years. This can be an extremely long time to wait to determine whether the product is acceptable, and a quicker turn around is usually desirable, but the latter may be impracticable or give rise to anomalous results.

Reference to the current specifications shows that most require the PCBs to be subjected to a test exposure time of 264 hours (11 days), a figure which the authors have also found (2b), with certain reservations (see below), to be a reasonable compromise between speed of results and accuracy of results.

Measurement Frequency

Test specifications typically require that the measurement of the surface insulation resistance be carried out on an infrequent basis, perhaps only three or four measurements in total. This can provide misleading results and fail to highlight vital evidence of potential field failures. For example, a board may be classified as a pass since it exhibits an acceptable SIR value at the end of the (possibly arbitrarily chosen) test duration. However, the data may have been insufficient to show that since the SIR values were decreasing rapidly with time, a similar test a short time later would have resulted in a failure i.e. the data were not sufficient to allow a full interpretation of the results. Similar considerations apply to other cases e.g. of boards whose SIR values either increase with time (see Section 5) or remain constant, albeit just less than that required by the test method. Thus a knowledge of the temporal variation of the SIR values is as important as its ultimate value. The more frequent the measurements the more information is available, and the quicker the user will be aware of any trends. It is our experience (2b) that trends can usually be detected from measurements made at hourly intervals. The growth and destruction of dendrites have been observed from "continuous" measurements i.e. every few minutes.

A reasonable compromise between time and speed for trend analysis is achieved by making measurements every hour.

Summary: *For meaningful SIR testing, the test conditions (e.g. temperature) must be chosen to avoid incurring any failure mechanisms unrelated to those experienced by the product in the field. The humidity should be as high as commensurate with good control to avoid condensation - 85% is recommended. The combination of bias voltage and inter-track spacing must ensure that the voltage gradient is similar to that experienced in the field, and certainly well below the substrate breakdown voltage. The duration of the test and number of measurements made, should be appropriate for the objective of the test; typical*

compromise figures recommended are - test duration 264 hours, with measurements made at hourly intervals.

3.4 Methods of Connection

Once the test board has been assembled connections for bias and measurement must be made for the SIR test to be carried out, and these can be the source of contamination which could easily affect the SIR test results. These connections consist of two parts, viz (i) the wiring from the monitoring system to the test fixture, and (ii) the actual connector that links the PCB to the test fixture wiring.

3.4.1 Wiring from Monitoring System to Test Pattern

There is a range of options available from the simple expedient methods appropriate in cases where only a few connections need to be made, to the more complex that are required for several hundred connections. Usually smaller gauges of wire are used to make the connections directly to the test PCB, to ensure that an excessively large weight of test cable does not drag the PCB out of its position within the test chamber. If the wire is of the multi-stranded variety then it will be more susceptible to oxidation than a single stranded wire, and also prone to drawing contaminants up the inside of any insulation by capillary action. However, the failure of any one individual strand of the wire will not result in the complete loss of that pattern as would happen if the sole conductor of a single stranded cable broke.

If the connections to the test patterns are made using a large number of unshielded small gauge (single or multi-stranded) wires then it is possible that the wiring loom will become entangled (poor test practice). More importantly, the variation within the current measurements may be greater than the values being measured resulting in poor quality data. Where only a small number of connections are required it may be feasible to use some form of coaxial cable in which the outer sheath is permanently grounded. However, this approach rapidly becomes inappropriate as the number of connections rises. In this case the use of a ribbon cable is more practical, while providing a ready made method of organising the wiring loom. Possible signal oscillation can be reduced by grounding every other wire in the ribbon cable and carrying this through to the guard bands on the actual test PCB.

The insulation materials of the cables themselves, are also a possible source of contamination of the test chamber. Failure to select the appropriate insulation material may produce extremely poor SIR results as the test PCBs become contaminated from this source during the test. To this end cables with PVC and other materials containing mobile halogens should not be used within the chamber. There are many polymeric materials available that are suitable, but one commonly used for the wiring within the actual test chamber is PTFE. Although this material has very good dielectric and insulation characteristics it is expensive (especially in ribbon cable form), it softens at elevated temperatures, and is susceptible to damage. To reduce the cost the cable can be broken into two segments; that which runs from the electrical test system to the exterior of the test chamber, where it is connected to the PTFE cable that enters the test chamber and is connected to the test PCB. In this way the length of PTFE required can be significantly reduced although additional intervening connectors are required. Recently, proprietary halogen-free insulated ribbon cables have become available at a fraction of the cost of PTFE which allows the intervening connectors to be omitted.

When dielectric materials are rubbed against each other small (triboelectric) currents are

produced. These currents are of the same order as the leakage currents being measured. In order to avoid this effect care must be taken to ensure that once the test is under way the cables are fixed in position with respect both to the chamber and to each other. This is another point for which the use of a ribbon cable wiring loom is of great assistance.

Summary: *For both good connections and minimising contamination it is recommended that ribbon cable should be used. Materials containing mobile halogens (e.g. PVC) must never be used in the test chamber.*

3.4.2 Connections to the Test PCB

There are several options available ranging from the simple expedient methods appropriate when the PCB is of a standard design, to the more complex for which design considerations must be made at an early stage. The choice will also be influenced by the size of the test population. It is imperative that SIR leads/connections should not contribute to sporadic failures (i.e. open circuits) which would complicate the SIR data obtained. In addition, SIR test lead connections should, if possible, be removed from contaminated areas, and attached in ways which reduce or eliminate the potential for contamination. The preferred method is soldering, although other options are available.

Soldering

Nearly all SIR test specifications detail an acceptable method of soldering wires directly to the actual test board. This operation can add further contamination to the PCB after it has undergone normal cleaning (if any) immediately prior to the measurement stages. This point is recognised in most specifications in that there is a requirement either to use a residue free/no clean fluxed solder, or to carry out a post-mounting, localised cleaning of the PCB in the region of the new soldered joints. Both these methods have a potential drawback. If the failures result from the SIR test, it is often difficult to attribute unambiguously the cause to either the original flux, or to the flux used in the attachment of the measurement wires. Whether the board is a genuine SIR test failure may therefore not be known.

Single Connectors

The most obvious example of this type of connector is the use of crimp terminals. These ensure good connection but are useful for only a single test, in that they must be removed from the wire at the completion of the testing and replaced. Their use is thus time consuming for fitting large numbers of test patterns.

An alternative is some form of spring loaded clip to make contact to the test board. However, there needs to be a suitable post on, or land at the edge of, the board to which to make contact. In addition, the clip would need to be clean and the surface protected (e.g. Ni or Au plated) and steps taken to eliminate the possibility of the clips shorting together due to unexpected movements. The latter might be achieved by using a plastic cover (halogen-free and precleaned) over the body of the clip. It has been found by the authors (2b) that prolonged exposure to elevated temperature can also result in relaxation of the connector system leading to a reduction of the contact pressure and ultimately to the clip becoming detached from the contact, especially if the chamber is subjected to some form of vibration such as the motor of the air circulating fan.

Multiple Connectors

A wide range of connectors is available and can be considered for use. Those which require the

addition to the test board of a mating half (e.g. standard IDC plug) may introduce their own sites of potential failure (residue trapped under the connector body), although they are capable of being used where a large number of test connections is required.

If the board is custom designed then provision can be made for the use of board edge connectors, either single or double sided. However, in either case shorts may develop within the connector between the card edge fingers. Further potential drawbacks are that if the testing is carried out over a prolonged period at an elevated temperature (1000 hours; 85°C) then there may be thermally induced relaxation of the contacts themselves resulting in a false high resistance reading as a result of an open circuit. The connectors may also act as moisture traps producing unexpected and unrequired leakage paths. Instead of card edge connectors an array of spring loaded probes could be considered. These would not provide these leakage paths. However, the probes would need to be rigidly fixed with respect to each other and this system could be expensive and complex for large numbers of contacts.

It was emphasised above that the use of insulation containing mobile halogen for wires within the test chamber is highly undesirable. Similarly, care must be exercised over the connector body materials. These must also be free of mobile halogens and cleaned prior to each use since the connector could easily pick up contaminants from handling outside the test chamber during the process of attaching the appropriate measurement and bias connections to it.

If these limitations are recognised and taken into account, then the use of connectors does provide a quick method of attaching large numbers of test patterns to the appropriate measurement system. They may be used more than once and are reasonably secure.

An Alternative Method for Limited Numbers of Connections

In view of the limitations concerning the above methods the authors evaluated a number of alternative methods of making reliable contamination-free connections to test boards (2b).

The most successful was particularly appropriate for small numbers of connections and could be applied to a test board or to actual product provided certain provisions were made. The patterns to be tested were connected to lands on the PCB (such as those suitable for card edge connectors) via tracking on the PCB surface. Prior to final cleaning solder bumps were formed on these lands. The PCB was then processed in the normal way. The ends of the wires to be connected to these lands were bared, tinned and cleaned. When the connections were ready to be made the solder on the PCB land was reflowed and the wire end inserted. The result is essentially a cast joint and has the advantages over normal soldering in that there is no flux residue at this point and that no additional provisions are required other than a land to which to solder.

An Alternative Method for Large Numbers of Connections

The use of connectors is extremely desirable where large numbers of connections are required not only because it simplifies the act of making the connections to the PCB, but also facilitates the sample to measurement system cabling. All the methods detailed previously are usable with care and have their own advantages and disadvantages. However, some of the disadvantages can be minimised by taking some further action. For example;

- if the standard spring contacts in card edge connectors were replaced with "knife blades" that actually cut into the contact land on the PCB, then there would be no possibility that thermal relaxation would cause an open circuit.

- to overcome the possibility of the PCB surface within the connector providing a leakage path this material could be removed by routing, thereby creating a crenallated card edge in the region of the connector.

- the spring loaded contacts could be replaced with screw down terminals and a locking system.

These possible methods do require some additional preparation of the PCB and do have their own limitations, but they do provide solutions to some of the existing problems.

Summary: *For reliable SIR testing care must be taken to ensure good contacts without incurring (i) extra soils, (ii) parallel leakage paths, or (iii) loss of continuity. Many options exist and the choice is one of "horses for courses".*

3.5 Test Procedure

The manner in which the test is carried out is as important as the sample preparation. Having expended considerable effort to ensure that the test samples are truly representative, and the test equipment is sound, further care is required to ensure that the results obtained are not compromised by avoidable procedural errors, which with pre-test planning can be avoided.

Whatever the connection method selected the samples should be mounted vertically within the test chamber, which should itself be clean and free of possible contaminants. If necessary drip/condensation shields should be fitted to prevent moisture droplets forming on the PCBs under test. Water drips can cause failures (2b). The bias voltage should be applied once the samples are ready in the test chamber prior to raising the temperature and humidity. Thus SIR measurements can be made at ambient conditions, and then subsequently throughout the ramp to the test conditions, under test conditions, and if required, after the PCBs have been returned to ambient after testing, in order to assess whether there has been any permanent change/degradation. The temperature should be raised ahead of the humidity and time allowed for the PCBs to come to thermal equilibrium to prevent condensation on the surface of the substrates.

Summary: *The test procedure must ensure a sensible test sequence to avoid, for example, condensation or bias application at high temperature. The recommended sequence at the start of the test is: bias applied; temperature raised to equilibrium; humidity raised. The order is reversed at the end of the test.*

3.6 Electrode Bias During Test

The majority of the test procedures use a bias reversal stage immediately prior to the SIR measurement. Consideration of the processes taking place during the SIR stress stage indicates that the total current flowing consists of three separate parts. These are:

- A. Electronic (drift) component,
- B. Ionic drift component,
- C. Ionic diffusion component.

The first two are in the direction of the applied field, whereas the third is in the direction of the concentration gradient. During much of the normal stress bias stage, © will be in opposition to (a) and (b) - the positive ionic species will have been drifted towards the negative electrode; the concentration gradient will be away from the negative electrode.

On reversal of the bias for the measurement stage, the first two components will instantly (ignoring transient capacitance effects) change sign, but the third will continue in the same direction as before. Thus, at this the measurement stage the three components will be additive. The total current is thus increased, and it is thought that this is precisely the original reason for the choice of reversal of bias. At the time that most of these tests were generated, measurement of low currents was difficult and anything that increased the available current was considered worthwhile. But this has a significant drawback in relating these measurements to the actual electrochemical processes involved. In practice, it means that it is always the peak ionic current which is measured. The decrease in the total current that occurs with time, the essence of the physical situation, is therefore not monitored. However, modern instrumentation is such that measuring very small currents is no longer a major problem. Hence measuring SIR values without alteration of the essential physical/chemical processes involved is now relatively straightforward.

If the bias is reversed, large currents will flow, which in the absence of limiting resistors, will inevitably result in the fusing/vaporisation of any dendrites which may have formed. Thus the end-point of some reliability tests will be markedly altered by the measurement technique imposed. Unfortunately, the majority of the current SIR test specifications regard the growth of dendrites as an anomaly and discount results associated with their occurrence, thus throwing away significant reliability data. *Bias reversal is therefore not recommended.*

The comments discussed above (Section 3.3) regarding the application of realistic voltage gradients and measurement frequency, are again relevant here.

Summary: *For meaningful SIR testing, there should be no reversal of biasing prior to measurements, the bias-inter track spacing combination should give realistic field gradients, and measurements should be made at least at hourly intervals. In addition, the measurement circuit should include sufficient series resistance to eliminate the possibility of destroying dendrites.*

3.7 Method of Leakage Current Measurement

Traditionally the insulation resistance for SIR testing has been measured by applying a large voltage (up to 100V) and measuring the resulting current using a high quality ammeter. The use of such a high voltage was required in the past, mainly because of the large inter-track spacing of the SIR pattern, and by the difficulty of measuring low currents. Hence the use of high voltages was the only feasible way to determine high resistance values. Additionally, it was considered desirable to have an accurate and precise measure of the resistance, further reinforcing the view that as large a current as possible should be induced.

In practice, precise knowledge of the insulation resistance is not required. What is important is a measure of the order of magnitude of the resistance values and resistance changes. This is most conveniently determined by measuring the logarithm of the current passing, and a good indication of the processes occurring can easily be appreciated without the necessity of recourse to using unreasonably high applied voltages. This reinforces the argument (e.g. in Sections 3.3 and 3.6) for a low bias voltage to provide realistic voltage gradients.

Measurement of the current can conveniently be made using a very low voltage drop current measuring equipment inserted into the bias circuit at the earthy end. This can be achieved most easily if the front-end of the current measuring equipment has a virtual earth amplifier input. The arrangement has been investigated and validated (2b) and is now incorporated into the GEC Auto-SIR instrument (18) specifically designed for SIR test monitoring. The GEC Auto-SIR also benefits from its ability to multiplex the measuring circuit round a large number of samples, whilst holding the earthy ends of all samples at (or very near to) ground potential. The complete instrument consists of a logarithmic current meter capable of measuring down to a few pA, and capable of cycling rapidly through a complete set of patterns in a short time under computer control. It is thus able to measure the changes occurring in the samples at frequent intervals throughout the test schedule.

Summary: *During SIR tests the current should be measured at virtual earth so as not to disturb the current flow.*

3.8 Pass/Fail Criteria

There are two methods of collecting and analysing the data, viz discrete measurements applying a pass/fail criterion, or analysing continuously (or frequently) collected data (see Section 3.3).

The pass/fail criterion varies from specification to specification. In some cases it is achieved by the user selecting a predetermined resistance value that must be exceeded by the test specimens at the end of the environmental exposure. In other cases a comparison of the final resistance with the initial resistance or with the resistance of a control group of test specimens, is required. Such variations are understandable and necessary, and it is essential that, prior to establishing a pass/fail criterion, there is a thorough understanding of the way in which the results will be applied. For example, digital circuits using high currents will require a very different pass/fail criterion to that required by high impedance, low current, analogue circuits. A very small leakage current may be critical in the latter but trivial in the former.

In all cases the provision to carry out a visual inspection pre- and post-testing is considered advisable and may permit the user to relate physical appearance with performance.

If the technique of continuous or frequent monitoring is employed (2a) many of these problems are eliminated, and a more precise and accurate picture of the likely defect rate is obtained. Work reported by McGuire (15) has shown that pass/fail data offer only a gross estimate of process yield, and that very large sample sizes must be taken to compensate. Data from continuous monitoring, although more complex to obtain and analyse, provide (19) much better differentiation between SIR test performances and hence provide a much better probability of predicting true defect rates. In addition, the technique of continuous monitoring makes it possible to separate IONIC and ELECTRONIC condition contributions (2a, 18, 19) to any leakage current, by the use of a complete current-time SIR curve. Base-line effects due to the intrinsic quality of the substrate can therefore be distinguished from the effects due to ionic contamination from the assembly process. Continuous monitoring is a feature of some state-of-the-art SIR testers (e.g. the GEC Auto-SIR instrument).

Summary: *For sensible SIR testing using a pass/fail criterion, the latter must be chosen carefully, and be appropriate to the objective of the test. Analysis of data from continuous monitoring is more meaningful and will be more cost effective over the product life cycle,*

and is therefore to be preferred.

4 A COMPARISON OF ELECTROMIGRATION AND SIR TESTS

Surface insulation resistance is a direct measure of the electrical leakage, which could affect circuit performance, and it may indicate the presence of contamination, which could cause long-term reliability problems by such mechanisms as electrochemical migration (ECM). SIR tests have long been the industry standard for assessing the corrosion-related reliability performance of soldering fluxes for electronic applications (20-23). However, as the adoption of finer pitch geometries and no-clean technologies has increased there has been an increased interest (24) in ECM, and comparisons have been carried out (3, 24) of instrumental parameters and test conditions.

ECM is the growth of conductive metal filaments under the influence of a DC voltage, and can occur on the surface of the board or through the bulk of a composite (e.g. paper-phenolic laminate); ECM tests are discussed in reference 25. Dendrite growth is by electro-deposition from a solution containing metal ions which are dissolved from the anode, transported by the electric field and redeposited at the cathode (see Figure 5). For ECM to occur, therefore, there are three conditions, viz ionic material, water, and an electrical potential between electrodes.

It should be noted that the migration referred to (17) in Section 3.3 differs from classic ECM dendritic growth in three ways: the migrating metal is copper, not lead or tin; the filament growth is from anode to cathode; the filament is composed of metallic salt, not neutral metal atoms.

The conditions of the ECM method (temperature, time, humidity, test pattern style etc) are similar (25) to those of the SIR method but the test is targeted specifically at evaluating failures caused by electrode material transport and subsequent growth of dendrites, not merely at measuring leakage currents. Typical test parameters are:

SIR IPC-SF-818 Class 3 Test 100V; bias -50V; 85°C; 85%RH; 7 days;

ECM Bellcore TR-NWT-000078 Test 100V; bias 10V; 85°C; 85%RH; 21 days;

The only major differences in the test parameters appear to be:

- (i) the level of applied bias; the latter has traditionally been higher in SIR tests, but with the trend towards reduced track width/spacings, continued use of these higher voltages is now being questioned in terms of effective voltage gradients and substrate breakdown voltages (see Sections 3.3. and 3.6).
- (ii) the requirement of the SIR tests to increase and reverse the bias voltage immediately prior to measurements: the requirement for bias reversal is also now being questioned (see Sections 3.6 and 3.7).
- (iii) the inclusion of current limiting resistors in the bias and measurement circuits of the ECM tests to prevent the destruction of dendrites due to high voltage and unrestricted currents. NB. It is common practice in SIR tests to discount any results

associated with the formation of short circuits (dendritic growth) between the comb tracks. Many SIR tests require that data associated with dendrite growth are ignored. The requirement for retaining any dendrites was discussed in Section 3.6. But it should be emphasised that all SIR data should be used in assessing SIR tests, unless the failure is unambiguously attributable to unrelated failure modes emanating from non-representative tests.

Recent work (24) comparing the two test methods using halide-free no-clean fluxes, has suggested that whilst the SIR test is more sensitive to the variation of flux chemistries, the ECM test appears to be more realistic. In the case of rosin-containing fluxes, both tests appeared to be equally informative, the insulation resistance being a function of the pH value of the flux. In the case of low residue no-clean fluxes, the SIR test was more stringent than the ECM test, the latter producing no failures. The SIR failures were attributed to the (high) 50 volt bias used in the SIR test (cf 10 volts bias in the ECM test). It was suggested that these failures would not have occurred under normal application conditions of ~5V.

If the changes in the SIR test method/parameters suggested in this report are undertaken, then the differences between the two tests would be minimal and the two tests would converge.

5 THE WAY FORWARD: A DISCUSSION

With the advent of newer soldering technologies, finer pitch devices, new solders/fluxes etc, it is necessary to review whether or not traditional SIR tests are still appropriate, and if not, in what ways should they be modified. The Sections above have indicated that these changes in technologies and/or materials do necessitate some changes if the test is to be continued to be used as a meaningful way of assessing service performance.

Consequently, the SIR test method needs to be revised from those of current specifications to take account of some critical areas of the test discussed above:

- * test board and pattern
- * test sample preparation
- * test conditions
- * test procedures
- * test measurement methods
- * test data collection and analysis

The most important of these is arguably the test conditions, and it is appropriate to discuss these further.

With regard to the electrical conditions of the test it is necessary to ensure that the choice of bias voltage and inter-track spacing provides a field strength which is not excessive, which simulates service conditions, and which is well below the dielectric breakdown of the sub-strate material. It would perhaps be better to quote a maximum field strength rather than inter-track spacings and bias voltage, and this is strongly recommended. In addition, with modern instrumentation bias reversal is no longer necessary to ease the measurement process. Its removal will also make the test method more realistic in terms of the actual chemical processes involved, and will ensure that any dendrites grown (a possible end point of any leakage) will not be destroyed or ignored.

Ignoring dendrites is to disregard an essential part of the physical/chemical processes involved and will lead to misleading results and ill-founded data. On several occasions (2b) the authors have examined boards, failed in service, which have been passed to military standards (i.e. any results associated with dendrites would have been ignored), whose very failure mechanism has been that of dendritic growth. Photographs of typical dendrites grown during SIR tests are presented in Figure 5 and amply demonstrate (i) how essential it is to take account of them in interpreting SIR test data, and (ii) how necessary it is to inspect the boards visually for complete appraisal of the tests.

If these two suggested changes (no bias reversal, sensible field strength) are incorporated into the test method the differences between ECM and SIR tests would be minimal. Indeed, current ECM tests are close to what the authors believe would be a truly representative test for SIR on modern boards.

In the case of humidity and temperature there is an apparent conflict. On the one hand they should be as high as possible to provide high acceleration factors to minimise the test time. On the other hand, they should not be so high as to induce anomalous performance through unrelated failure mechanisms. These factors should be kept in mind when selecting appropriate test conditions. Humidity levels should never exceed 90% and even this value may be too high unless careful control and monitoring are exercised. For this reason the authors believe that 85% RH is the most appropriate level.

Temperatures should certainly not exceed 85°C, and even this value is now questionable under certain circumstances such as the evaluation of no-clean fluxes. No-clean fluxes usually contain weak organic acids (e.g. adipic, glutaric) instead of the rosin as the activator. Even though these acids may behave differently from the rosin acids, the SIR test has been used to evaluate no-clean fluxes. In 1993 Sohn (12) suggested that some SIR tests may be inadequate in assessing the long-term contribution of flux residues to product performance. In particular his results indicated that SIR testing at 85°C (in 85% RH) resulted in volatilisation/degradation of the activator used in the no-clean fluxes. This implied that the SIR test was inducing changes unrealisable in service, compromising any assessment of product reliability based on testing at this temperature. Other results suggested that SIR testing of water-soluble fluxes at 85°C may also be compromised.

Further work by Lei and Ramirez (11) supported these suggestions. That work indicated that there may be at least three reactions occurring simultaneously on the SIR pattern involving the flux residue : (a) evaporation of the adipic acid (i.e. dicarboxylic acid), (b) dissociation/polymerisation of the adipic acid, and (c) corrosion of the copper tracks. All three processes consume adipic acid and contribute to the anomalous SIR values obtained. At 75°C and above, 90% of the flux residue was removed in 8 hours. Qualitatively the humidity appeared a less significant factor than the temperature on the flux reduction rate. These results indicate that 85°C/85% RH is not a proper acceleration condition for long term low solids, no-clean flux reliability assessment, and it was concluded that a more appropriate acceleration test condition would be 50°C/90% RH for 168 hours. At this condition 75% of the original flux residue remained on the board at the end of the test.

In view of the fact that it is possible that the majority of future fluxes may be of the low-solids no-clean variety (or water-soluble), the choice of appropriate SIR test environmental conditions is clearly of major importance. A suggested compromise, based on the evidence available at the present time, is:

(a) traditional liquid fluxes/pastes; board cleaned
Repsir4.doc

85°C 85% RH

i.e. same as Class 3 IPC-TM-650

(b) low solids, no-clean fluxes

50°C 85% RH

i.e. same as Classes 1 & 2 IPC-TM-650

Another potential drawback of SIR testing at 85°C was suggested by Sohn (12). He claimed that exposure to 85°C alters the material under test e.g. the hydrolytic stability of the solder mask, leading to SIR degradation. Other work (27) has also demonstrated that the inherent insulator material properties must be recognised as significant contributors to lower SIR values during elevated testing.

Clearly, none of the materials of the board or assembly processes can be considered benign. Hence SIR tests of the future must take into account the effects which materials may have on the implementation and/or the results of such a test. This may well result in using updated SIR patterns and modifying temperature, humidity, bias, etc to suit the particular system being evaluated. It will certainly make the test more representative of service conditions.

As has been mentioned earlier none of the current standards and specifications actually require or even make provision for the use of components. While this is adequate when the user is evaluating a specific part of a system (e.g. fluxes) it is clearly inadequate if the user is trying to qualify a whole process. All PCBs have components mounted on them and if the final assembly is to be cleaned then the components will affect the efficiency of this process by amongst other things trapping contaminants, retaining dirty cleaning fluid and masking areas of the PCB surface. A process may be qualified as acceptable on test coupons without components yet be totally inadequate to assess the final product. Components should be included on the test board.

Serious consideration must be given to the modification of the commonly used "standard" test patterns, to incorporate the more important of the points discussed in Section 3, in particular with respect to track spacing, guard banding and the ability to populate the board. There is an argument that there should be a UK standard pattern(s) and in this respect the patterns designed for the UK collaborative programme on evaluating CFC replacements (9) provide an excellent starting point.

Regarding the critical areas of test measurement method, data collection and data analysis many of the changes advocated in the Sections above (e.g. frequent or continuous monitoring as well as go/no go test mode, measurement of small currents, simultaneous measurements on many boards etc) require new test instrumentation. The latter are now becoming available. Indeed the GEC Auto-SIR has been specifically designed to incorporate many of these issues.

Finally, it is clear that much work still needs to be carried out in the whole area of SIR testing, and the proposed NPL shared-cost collaborative programme should provide much useful and relevant data.

6 RECOMMENDED FUTURE TEST REGIME

The Table below summarises the considerations detailed elsewhere in this report that are considered most appropriate for future SIR testing.

Parameter	Trials	Product Evaluation
Test Substrate	FR4, copper tracks, with solder resist, provision for components	Current Production
Test Pattern Style	Interleaved combs both beneath components and around device pads. All patterns to be guard banded by earth track.	
Test Pattern Design	Track widths and spacings of a maximum of 0.32mm or finer if required. NB Field strength is important.	Track widths and spacings that are representative of production.
Preparation	All items, test substrates and components should be cleaned prior to use (e.g. using a proven cleaning regime or an alcohol/water ionic extraction system).	Use the same system as that which is being evaluated.
Assembly	Standard infrared reflow or wave soldering techniques.	Use the same system as that which is being evaluated.
Sample Plan	A minimum of three examples of any test condition (more preferred) and a control group.	
Environmental Conditions	<p>Traditional fluxes/pastes 85°C; 85% Relative Humidity 200 hours extended to 1000 hours if time permits or if interim results indicate that it is necessary.</p> <p>Low solids no-clean fluxes 50°C; 85% Relative Humidity 200 hours extended to 1000 hours if time permits or if interim results indicate that it is necessary.</p>	
Measurement Frequency	Every hour for trend analysis Continuous for data on individual dendrite growth	
Bias Voltage	5V (NB appropriate voltage gradients are important) No reversal	Use the same voltage as that of the product which is being evaluated. No reversal
Pass/Fail Criteria	User definable e.g. related to maximum acceptable leakage	

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8 REFERENCES

In the course of this work a large number of standards, books, papers, reviews, conference proceedings etc, have been accessed. These, together with the results of many pieces of unpublished GEC work, have been used to distil the information and recommendations presented in this report. Apart from the references directly made in the text, other useful references are cited under the Bibliography.

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