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The Impact of Thermal Cycle Regime on the Shear Strength of Lead-free Solder Joints

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National Physical Laboratory
Teddington, Middlesex, UK, TW11 0LW

ABSTRACT

The purpose of this work was to undertake a comparison of accelerated test regimes for lead-free solders. Identical samples were subjected to six different regimes to investigate the effect of thermal excursions, ramp rates and temperature dwells. The most damage to joints was found to be caused by thermal cycling between -55 and 125^{o}C, with a 10^{o}C/min ramp rate and 5 minute dwells. Larger thermal excursions were shown to give faster results without compromising failure mode.

Similar degrees of damage to lead-free solder joints were experienced with thermal shock regimes with ramp rates in excess of 50^{o}C/min. However, these regimes, although faster to undertake, appeared to cause different crack propagation modes than the thermal cycling. However, the difference may be small and thermal shock testing may still be used to differentiate between or enable ranking of, process or material changes.

The results across all types of cycles showed very little difference in rates of joint degradation between SAC (95.5Sn3.8Ag0.7Cu) and SnAg (96.5Sn3.5Ag) solder alloys.

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National Physical Laboratory
Teddington, Middlesex, UK, TW11 0LW

Approved on behalf of Managing Director, NPL, by Dr C Lea,
Head, Materials Centre

CONTENTS

1 Introduction

Electronics assemblies are manufactured from a range of materials with different thermal expansion coefficients (TCE) – see Figure 1 for a cross-section of a typical joint. As these assemblies experience temperature/power changes during use (e.g. power consumption; switching equipment on/off; day/night temperature changes), the TCE mismatches cause strain and stress in solder joints, which creep and relax over time. Such strains can result in crack initiation (usually in the solder joint under the component), subsequent crack propagation through the solder fillet, and finally failure of the joint. The resistance to cyclic strains called cyclic fatigue resistance is a material property of an alloy and varies with strain range and strain rate (i.e. applied thermal load).

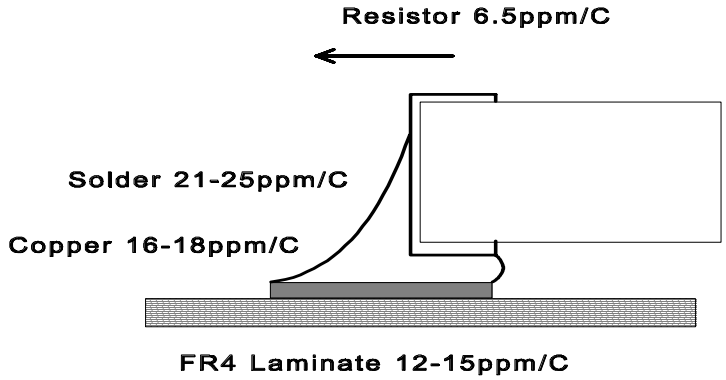

Figure 1: Schematic cross-section of a SM assembly highlighting the CTE (X-axis) mismatches.

Thermal cycling causes cyclic strains and develops cracks in a similar way to natural usage and weakens the joint structure by cyclic fatigue. Thermal cycling can therefore be conveniently employed in accelerated testing of the joint, to assess alloy reliability. The purpose of this work is to assess various thermal cycle loading regimes in terms of fatigue damage induced in a Pb-free solder joint. Although various thermal loading cyclic regimes have been developed over 40 years for Pb-based solders, these may not be applicable for lead-free alloys [Reference 1]. As the thermal-cycling is applied in wider temperature range than is generally the case in the field use, the loading is accelerated and an acceleration factor (AF) can be established. The acceleration factor is a ratio between the number of thermal cycles used in accelerated testing and the number of natural use cycles, causing equivalent damage in the solder joints. For Pb-free alloys, the AF may not simply be proportional to a temperature range as is the case for Pb-based alloys. Hence thermal-loading regimes used to evaluate reliability of solder joint have to be re-evaluated for Pb-free alloys.

To assess reliability and damage to the solder joint, a range of methods can be employed. There can be either destructive or non-destructive assessments. The non-destructive approach is to use continuity testing, and by analysing the response from a large number of joints with either lognormal or Weibull distributions, a failure prediction can be made.

However, the technique is dependent on complete electrical failure occurring, which can be a severe disadvantage when high numbers of cycles (2000-5000) may be required to reach sufficient number of failures.

The destructive methods do not require a complete failure for the damage level to be assessed, thus fewer thermal cycles are required. Two techniques commonly used are dye penetration and shear measurements. Dye penetration measures the fatigue in terms of a crack area and shear measurement gives maximum strength i.e. the force required to break the solder joint.

The work presented here uses shear measurement to assess the relative damage caused by a range of thermal cycle regimes.

2 Test Assemblies

2.1 Component Selection

When field failures occur in solder joints, these are generally in components which have a large thermal coefficient of expansion (TCE) mismatch with the substrate on which they are mounted. Therefore, this work concentrates on failures and failure modes within these component types, as these are the structures most likely to fail first in a field environment.

This work utilises ceramic chip resistors. These components are present in most electronic assemblies. Due to their alumina bodies, they have a TCE is much lower than in common substrate materials (see Figure 1), and hence are more prone to fail from cyclic strain damage accumulating in the joints. The magnitude of the effect is dependent on the component size. Three resistor sizes have been utilised in this work, R1206, R0805 and R0603. Being generally cuboid in shape with vertical sides, these components lend themselves to shear testing, and hence a measurement method of cyclic fatigue. Currently there are two widely available termination finishes for these components, Sn and SnPb. In the experiment described only the pure Sn component finish was used.

The component terminations were checked to ensure they did not contain any lead, since small additions of lead significantly alter alloy properties such as alloy strength [References 2 & 3].

2.2 Substrate Finish Selection

FR4 substrates with the ENIG finish were used in this study as they are Pb-free, in common usage and widely available from most PCB manufacturers.

2.3 PCB Design

The vehicle design used here contains three types of chip resistors as listed in table 1. Although incorporated into the design, the 2512 chip resistors were not utilised in this work. An example of a suitable PCB layout for shear testing and micro-sectioning is shown in Figure 2. This is fabricated from a single-sided FR4, thickness 1.6 mm, Cu thickness of 35 µm (Cu plating 1 oz/sq.ft) and immersion Au over electroless Ni (ENIG).

Table 1: List of components mounted on the test substrate

Component name	Component size [mm]	Number of component mounted on a substrate
R1206	3.20 x 1.60 x 0.06	13
R0805	2.00 x 1.20 x 0.06	13
R0603	1.60 x 0.08 x 0.06	13

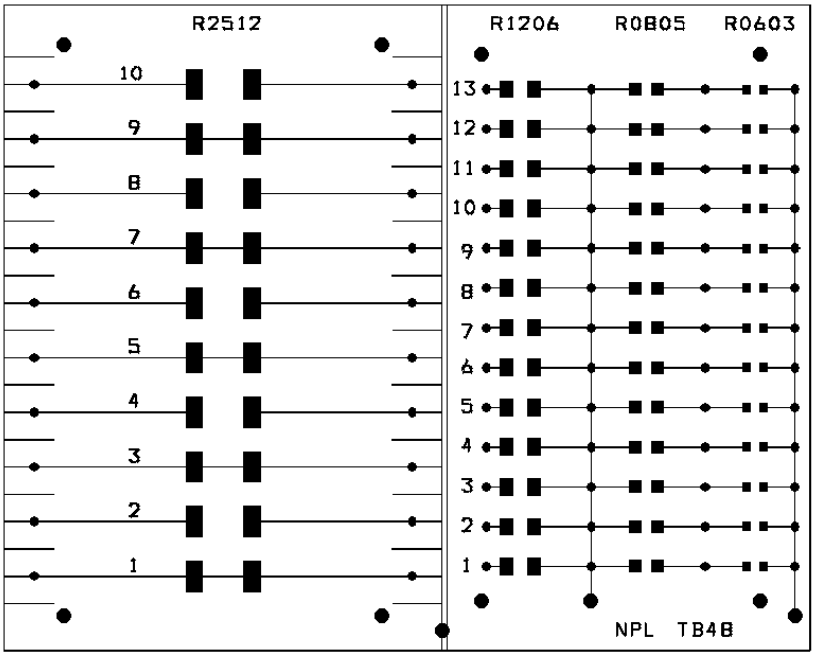

Figure 2: Test board layout (81 x 65 x 1.6 mm)

2.4 PCB Assembly

Substrates were stencil printed with solder paste using a stainless steel stencil with a thickness of 150 µm (0.006”). The pastes used were 95.5Sn3.8Ag0.7Cu and 96.5Sn3.5Ag. Components were placed onto the substrates using an automatic placement system. These processes ensured a regular solder joint volume. Reflow of the lead-free solder paste was achieved in a convection reflow oven and the soldering profile was measured at 5 different locations on the substrate as marked in Figure 3. Reflow temperature profiles are shown in Figure 4 and the time above 220 and 250°C is tabulated in Table 2 for each location.

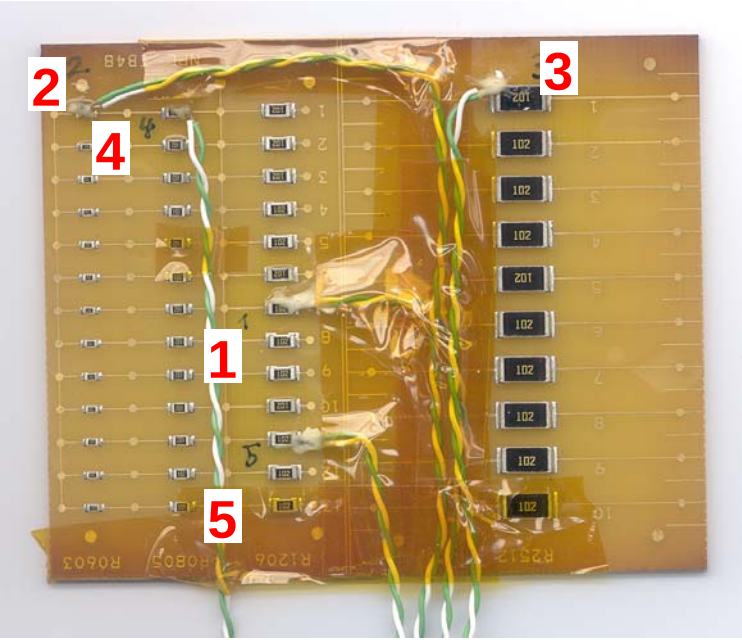

Figure 3: Location of thermalcouples prior to reflow profile measurement

Table 2: Typical reflow temperature profile for lead-free solders

Channel	Component	Time above 220°C	Time above 250°C
1	R1206 center	00:57	00:00
2	R0603 corner	01:21	00:55
3	R2512 corner	01:12	00:27
4	R0805 half way	01:14	00:26
5	R1206 half way	01:09	00:19

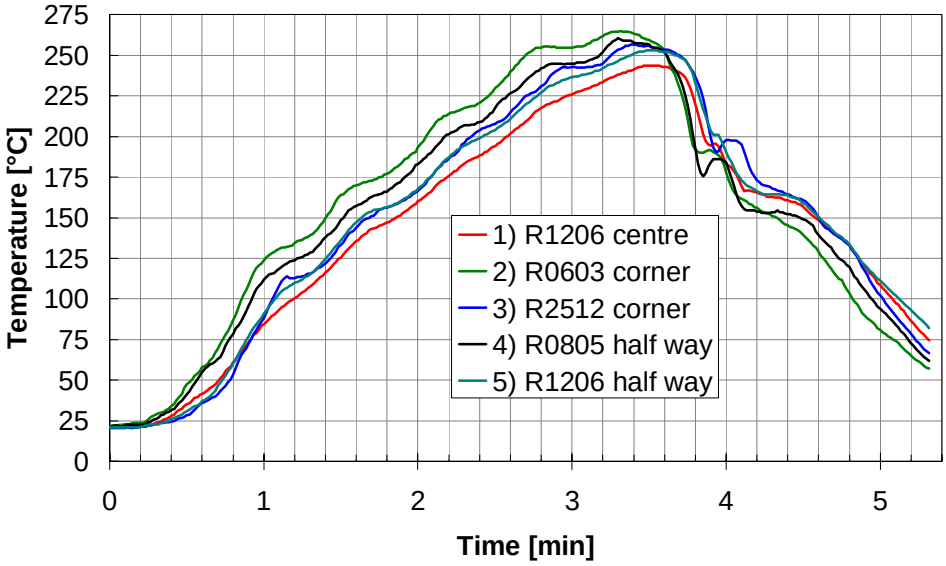

Figure 4: Reflow profile of the board assembly

2.5 Thermal Cycling

The choice of the cycling regime used to evaluate the reliability of lead-free solder joints is crucial as the relative performance of different solder alloys can change with thermal cycle parameters such as dwell temperatures and times, and the ramp rates between the dwell temperatures. The greater the temperature range and the larger the number of cycles, the greater the damage experienced by a solder joint. But it is vital that the regime selected should reflect the likely working environment of the product(s) of interest (e.g. military, automotive, consumer etc). In recent years the military and automotive sectors have preferred to use the same cycling regime (-55°C to 125°C), and this now appears suitable for many, if not all, applications. Table 3 lists thermal cycle regimes used in this evaluation study. Figure 5 shows a graphical representation of the thermal cycles.

Table 3: Tested temperature cycling regimes within ±4°C of the set value

Cycle	Low temp	High temp	Ramp	Dwell	Period
	[°C]	[°C]	[°C/min]	min	min
A	-55	125	10	5	45
B	-55	125	18	10	40
C	-20	125	10	5	40
D	-12	125	65	5	11
E	-20	80	10	5	30
F	-55	125	55	0	6.6

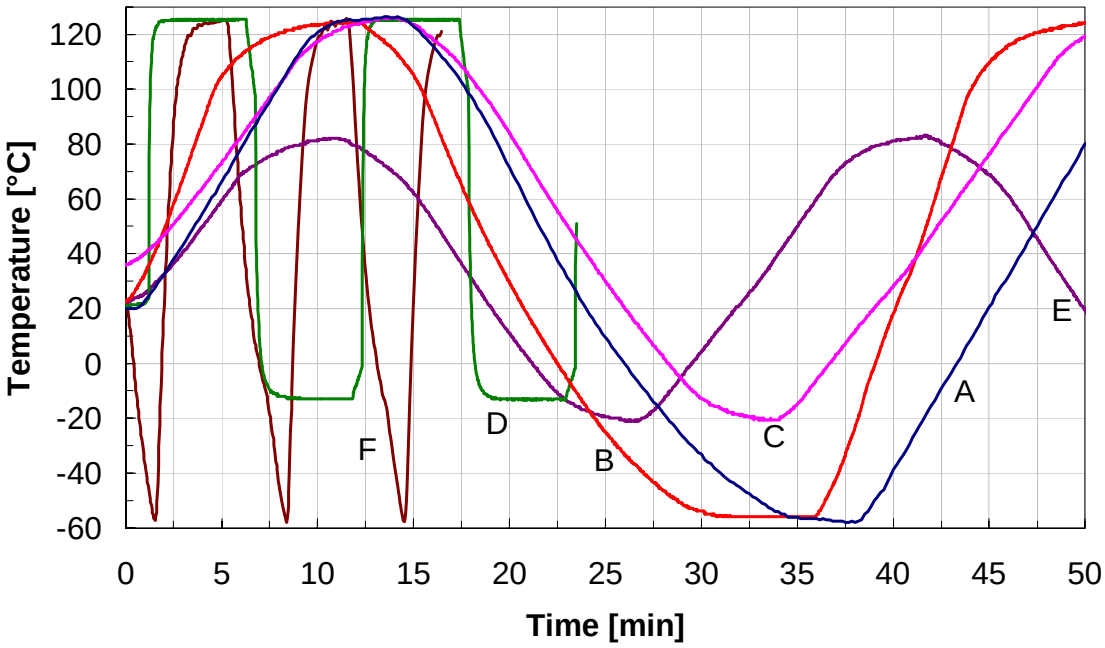

Figure 5: Thermal-cyclic regimes tested

2.6 Shear Testing

Shear testing is an established destructive method for evaluating not only the degree of crack propagation and damage to the solder joint, but also the general strength of the joint. The method is based on the assumption that the presence of a crack in the solder joint, its size and the extent of its propagation will influence the strength of a joint. Hence a correlation can be established between the strength of the solder joint and joint failures. Figure 6 shows a typical shear test. These tests were undertaken on a Dage Series-4000 modular multi-function bond-tester.

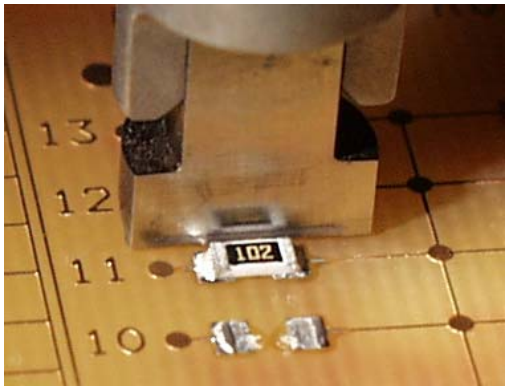

Figure 6: Shear test jig and push-off tool before a shear test

The following steps were carried out to assist shear testing:

- The substrate was cut into sections suitable for the shear tester holding jig, using a water-cooled diamond saw, which produces a clean edge with minimum stress to the board
- The sections were cleaned (e.g. with IPA - iso-propyl alcohol) to remove any contaminant residues from the cutting stage, and dried using compressed air
- The necessary test conditions were set, of which the most important is the stand-off height of the tool is equal to h/2 (typically 80 µm), between the bottom of the shear tool and board surface (h is the stand-off height between the component and the board surface)
- During each test, the shear tool was moved forward at a defined speed (200 µm/s) against the test component, and the applied force increased until the attachment was broken.

The data obtained in the test was analysed in terms of the ultimate shear force required to rupture the solder joint, and then plotted as a function of the number of thermal cycles to which the assembly had been subjected.

2.7 Micro-sectioning

Metallographic micro-sectioning was undertaken on selected samples. These samples were viewed both optically and in a scanning electron microscope.

3 Results

3.1 Data Interpretation

For each thermal cycling regime, 20 substrates were tested. Two substrates of each alloy were removed after every 300 cycles of each regime. On each substrate the ultimate shear tests were performed on 13 of each resistor type. An average value was calculated from the 26 individual measurements and plotted together with 1st and 3rd quartile of a box - whisker diagram shown in Figures 7 to 12.

The box-whisker diagrams reveal distribution of ultimate shear forces measured after reaching a certain number of cycles. Although the testing was performed at an exact number of cycles, the locations of boxes plotted in the diagram are adjusted sideways around the nominal number of cycles to avoid overlaying of data. Top and bottom side of the boxes indicate 1st and 3rd quartile (Q1, Q3) of the population sample. The line drawn across a box is indication of the median (quartile Q2). The vertical lines (whiskers) from these boxes extend to the last data point within the range of the limits. The upper and lower limit are calculated according to the relationship:

Lower Limit: Q1 - 1.5 (Q3 - Q1), Upper Limit: Q3 + 1.5 (Q3 - Q1)

The circle is the population mean and asterisks (*) are outliers (data points laying above the 4th quartile and below the 1st quartile).

3.2 Cycle A

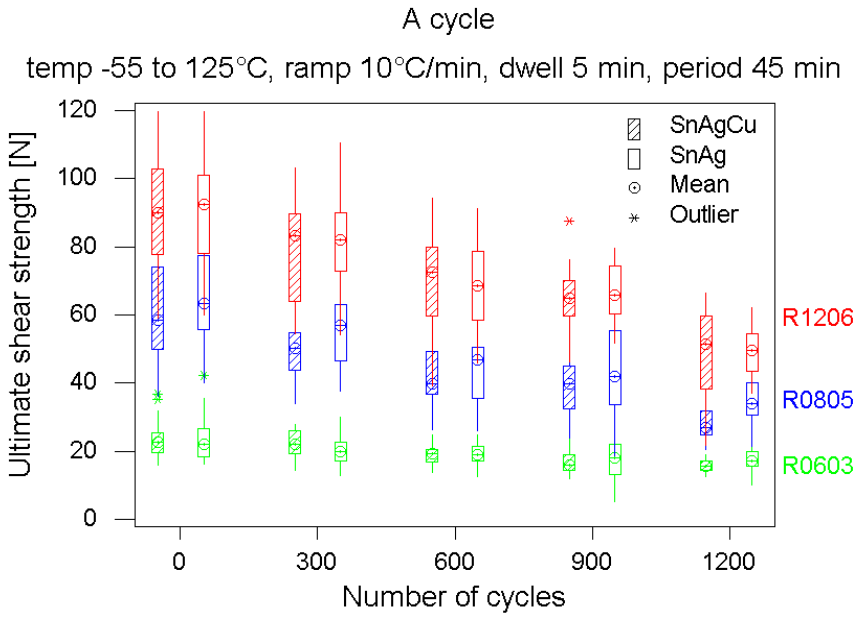

Figure 7: Cycle A – military applications testing

This is the common test cycle regime used in military applications testing, hence the wide temperature range of the cycle. The ramp rate of 10°C/min is a moderate ramp rate, slower than a thermal shock regime, which is typically above 20°C/min [Reference 4]. The relatively short dwell time of 5 min is to minimize cycle period. The USS results are shown in Figure 7.

3.3 Cycle B

This type of cycle is a common test regime used in automotive industry hence the wide temperature range of the cycle. The ramp rate of 18°C/min is a ramp rate just at the limit below the thermal shock region. The saved time on the ramps is compensated by prolonged dwell times of 10 min so overall cycle period is close to cycle A. The USS results are shown in Figure 8.

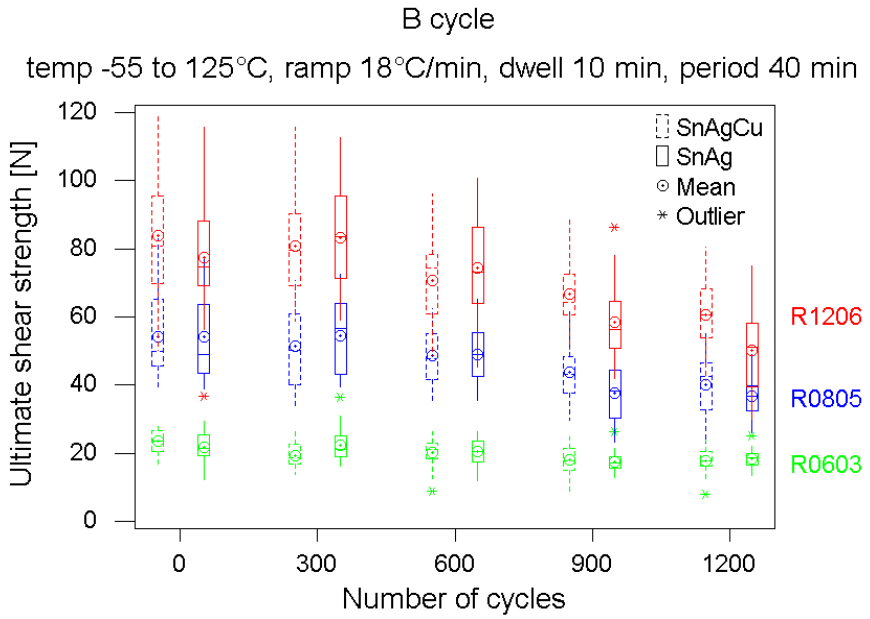

Figure 8: Cycle B automotive under hood testing

3.4 Cycle C

This type of cycle is a common test regime used in telecom electronics. The ramp rate of 10°C/min is a moderate ramp rate safely below that of a thermal shock regime. The USS results are shown in Figure 9.

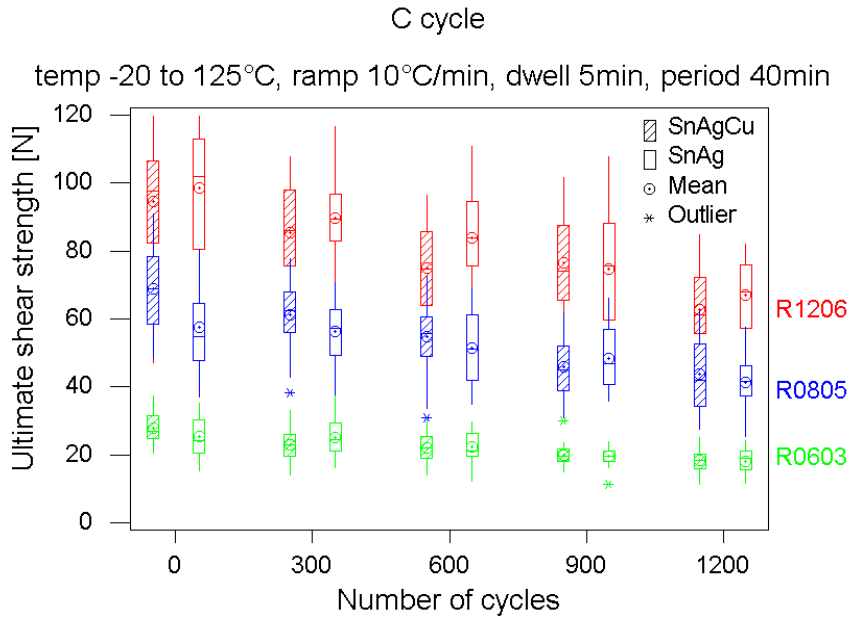

Figure 9: Cycle C automotive - avionics industry testing

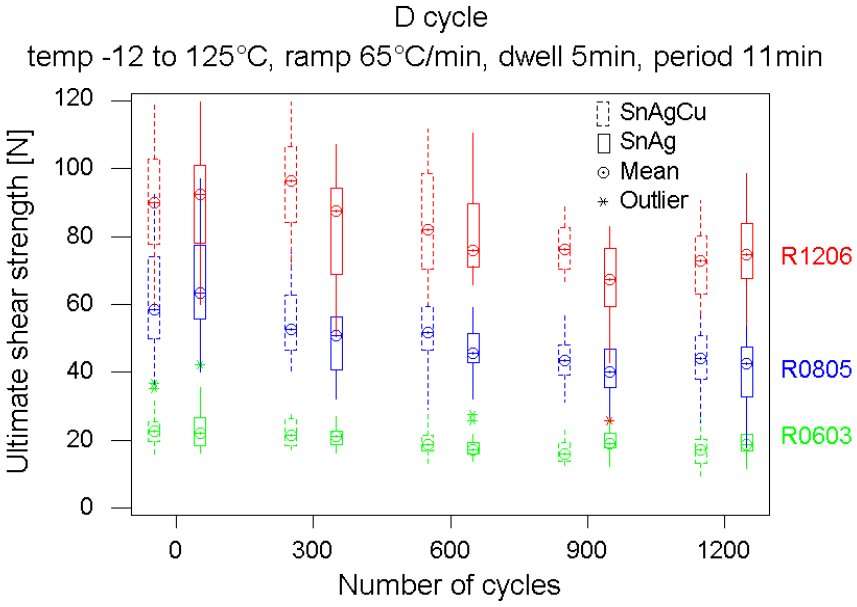

Figure 10: Cycle D liquid to liquid thermal-shocking cycle

3.5 Cycle D

This type of cycle is a common test regime used in automotive industry hence the extreme span of temperatures. The ramp rate of 65°C/min is a thermal shock regime and dwell times of 5 min make this much faster than the previous cycles.

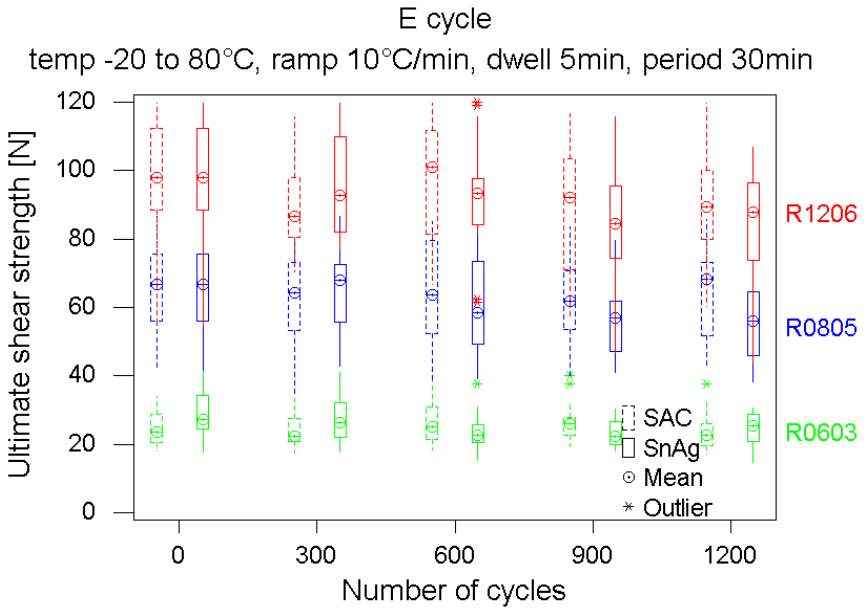

Figure 11: Cycle E consumer electronics thermal cycle

3.6 Cycle E

This type of cycle is very benign and is used in consumer electronics testing. The ramp rate of 10°C/min is moderate. The overall cycle period is intermediate between the short cycle of D and that of A.

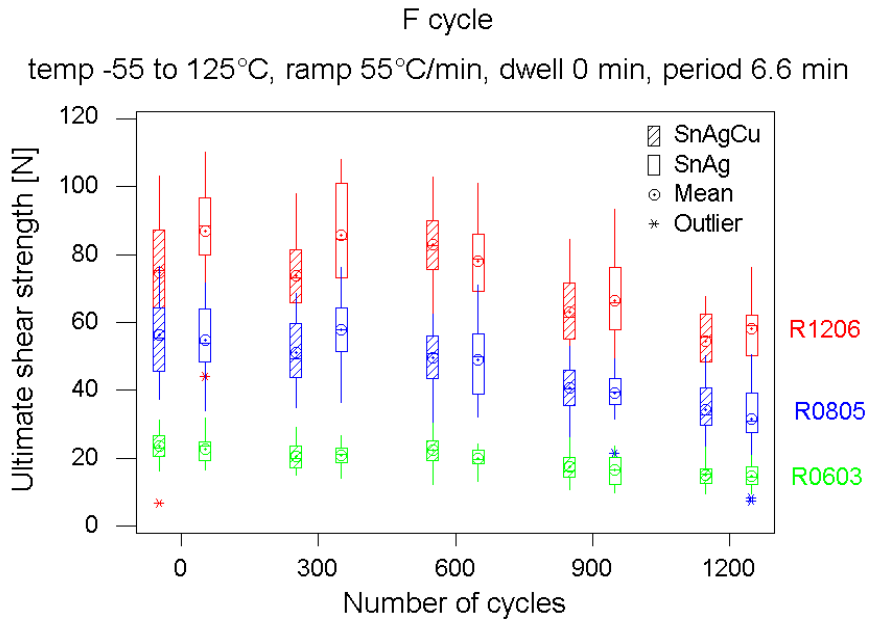

Figure 12: Highly accelerated thermal shock cycle (HAST)

3.7 Cycle F

This cycling regime is an example of a thermal shock regime. The damage in solder joints is not caused just by steep temperature ramps but also by temperature gradient between a substrate and components. This generates stresses, which can uncover short-term manufacturing defects in electronics.

3.7 Acceleration Effects

Table 4 shows the ultimate shear strengths for the two alloys after 1200 cycles of the 6 thermal cycling regimes. Numbers in brackets are percentage drops in USS compared to the USS at 0 cycles.

In Table 5, the columns titled “Acceleration effect” list linear slope approximation of the decrease in USS per cycle (in mN/cycle) between 0 and 1200 cycles. Columns titled “Acceleration effect/Period” show linear slope divided by cycle period. This is a economic measure of thermal cycling as it shows time to create damage in the two lead-free alloys for 6 different thermal cycles.

The acceleration effect and acceleration effect/period data is plotted graphically in Figures 13 to 16.

Table 4: Average declination of ultimate shear strength for 6 temperature cycles and two alloys after 1200 cycles

1206						SnAg	SnAgCu
Cycle	Low Temp	High Temp	Ramp	Dwell	Total Perio	USS0/USS1200 (%diff))	USS0/USS1200 (%diff)
	[°C]	[°C]	[°C/min]	[min]	[min]	[N]	[N]
A	-55	125	10	5	45	92 / 48 (-48%)	90 / 48 (-47%)
B	-55	125	18	10	40	77 / 50 (-35%)	83 / 60 (-28%)
C	-20	125	10	5	40	98 / 67 (-32%)	94 / 62 (-34%)
D	-12	125	65	5	11	92 / 75 (-18%)	90 / 72 (-20%)
E	-20	80	10	5	30	98 / 83 (-15%)	98 / 88 (-10%)
F	-55	125	55	0	6.6	87 / 58 (-33%)	75 / 54 (-28%)

0805						SnAg	SnAgCu
Cycle	Low Temp	High Temp	Ramp	Dwell	Total Perio	USS0/USS1200	USS0/USS1200
	[°C]	[°C]	[°C/min]	[min]	[min]	[N]	[N]
A	-55	125	10	5	45	65 / 34 (-48%)	61 / 28 (-54%)
B	-55	125	18	10	40	54 / 34 (-37%)	51 / 40 (-22%)
C	-20	125	10	5	40	57 / 41 (-28%)	68 / 43 (-37%)
D	-12	125	65	5	11	65 / 40 (-38%)	61 / 43 (-30%)
E	-20	80	10	5	30	65 / 55 (-15%)	65 / 64 (-2%)
F	-55	125	55	0	6.6	55 / 32 (-42%)	56 / 34 (-39%)

0603						SnAg	SnAgCu
Cycle	Low Temp	High Temp	Ramp	Dwell	Total Perio	USS0/USS1200	USS0/USS1200
	[°C]	[°C]	[°C/min]	[min]	[min]	[N]	[N]
A	-55	125	10	5	45	23 / 17 (-26%)	23 / 15 (-35%)
B	-55	125	18	10	40	21 / 18 (-14%)	23 / 17 (-26%)
C	-20	125	10	5	40	25 / 18 (-28%)	27 / 18 (-33%)
D	-12	125	65	5	11	23 / 18 (-22%)	23 / 16 (-30%)
E	-20	80	10	5	30	28 / 24 (-14%)	24 / 23 (-4%)
F	-55	125	55	0	6.6	23 / 15 (-35%)	24 / 15 (-38%)

Table 5: Effect of 6 thermalcycles on ultimate shear strength for two solder alloys after 1200 cycles

1206						SnAg	SnAgCu	SnAg	SnAgCu
Cycle	Low Temp	High Temp	Ramp	Dwell	Total Perio	Accelerating effect	Accelerating effect	Accelerating effect/Period	Accelerating effect/Period
	[°C]	[°C]	[°C/min]	[min]	[min]	[mN/cycle]	[mN/cycle]	[mN/cycle/min]	[mN/cycle/min]
A	-55	125	10	5	45	37	35	0.81	0.78
B	-55	125	18	10	40	23	19	0.56	0.48
C	-20	125	10	5	40	26	27	0.65	0.67
D	-12	125	65	5	11	14	15	1.29	1.36
E	-20	80	10	5	30	13	8	0.42	0.28
F	-55	125	55	0	6.6	24	17	3.63	2.56

0805						SnAg	SnAgCu	SnAg	SnAgCu
Cycle	Low Temp	High Temp	Ramp	Dwell	Total Perio	Accelerating effect	Accelerating effect	Accelerating effect/Period	Accelerating effect/Period
	[°C]	[°C]	[°C/min]	[min]	[min]	[mN/cycle]	[mN/cycle]	[mN/cycle/min]	[mN/cycle/min]
A	-55	125	10	5	45	26	28	0.57	0.61
B	-55	125	18	10	40	17	9	0.42	0.23
C	-20	125	10	5	40	13	21	0.33	0.52
D	-12	125	65	5	11	21	15	1.89	1.36
E	-20	80	10	5	30	8	1	0.28	0.03
F	-55	125	55	0	6.6	19	18	2.91	2.78

0603						SnAg	SnAgCu	SnAg	SnAgCu
Cycle	Low Temp	High Temp	Ramp	Dwell	Total Perio	Accelerating effect	Accelerating effect	Accelerating effect/Period	Accelerating effect/Period
	[°C]	[°C]	[°C/min]	[min]	[min]	[mN/cycle]	[mN/cycle]	[mN/cycle/min]	[mN/cycle/min]
A	-55	125	10	5	45	5	7	0.11	0.15
B	-55	125	18	10	40	3	5	0.06	0.13
C	-20	125	10	5	40	6	8	0.15	0.19
D	-12	125	65	5	11	4	6	0.38	0.53
E	-20	80	10	5	30	3	1	0.11	0.03
F	-55	125	55	0	6.6	6.6	7	1.00	1.07

Accelerating effect: $(USS_0\text{-}USS_{1200})/1200$
Accelerating effect/Period: $(USS_0\text{-}USS_{1200})/1200/T_{period}$

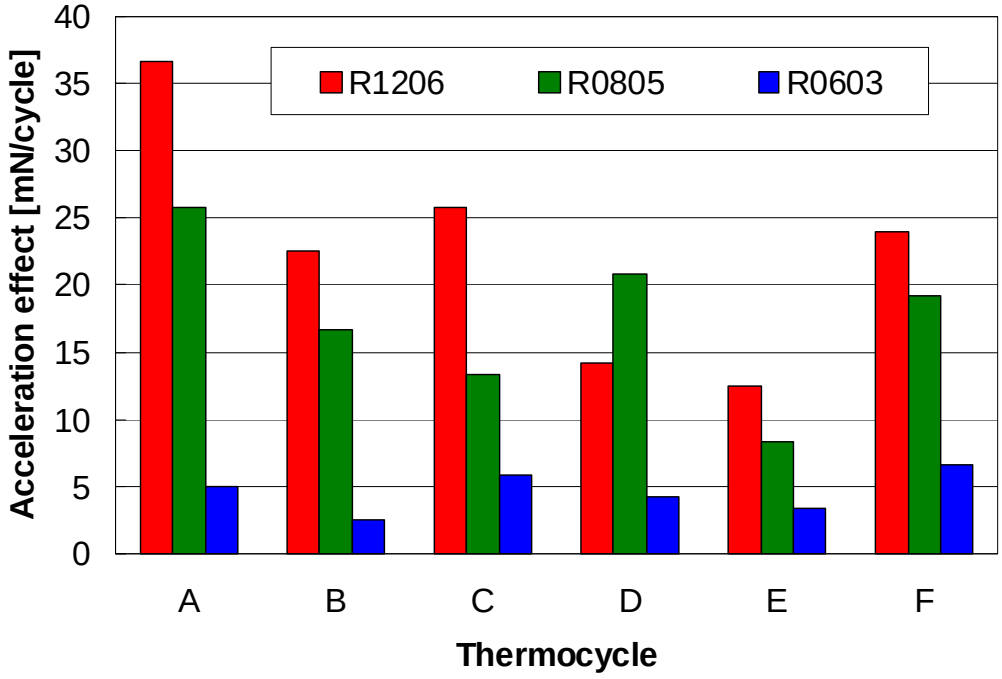

Figure 13: Performance of thermal cycles for SnAg solder alloy

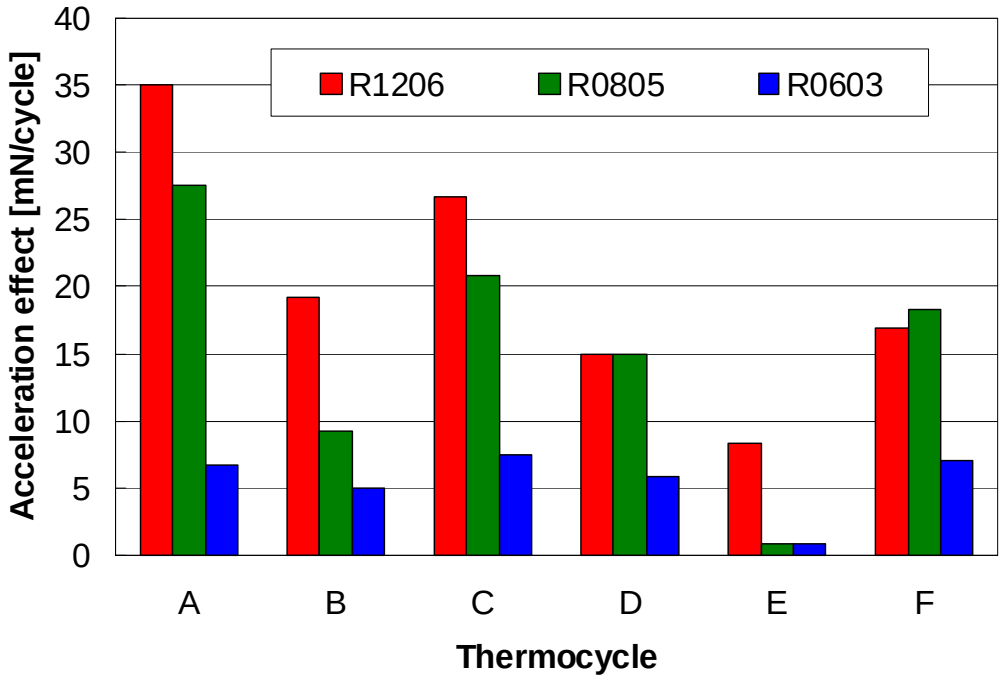

Figure 14: Performance of thermal cycles for SnAgCu solder alloy

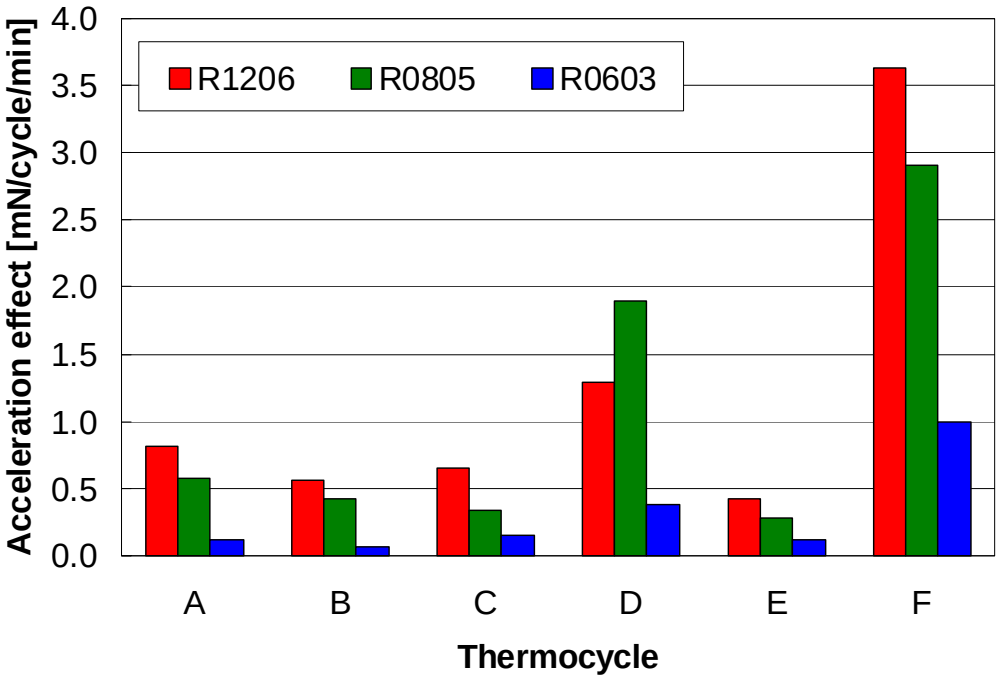

Figure 15: Performance/time of thermal cycles for SnAg solder alloy

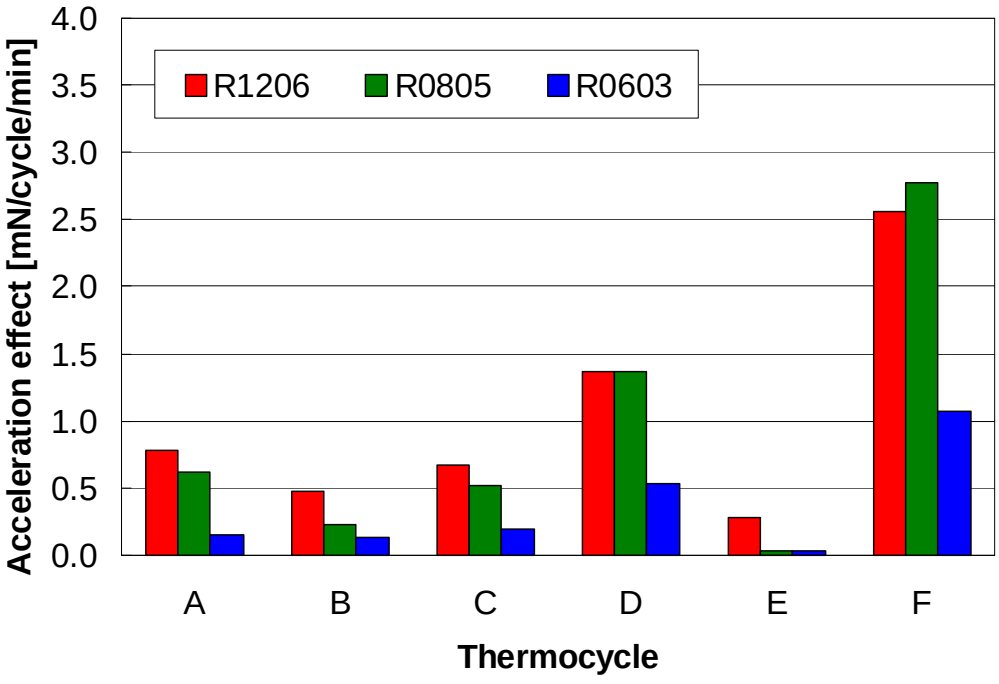

Figure 16: Performance/time of thermal cycles for SnAgCu solder alloy

4 Discussion

With all cycles (A to F), the ultimate shear force decreases with increasing number of cycles for both the SnAgCu and SnAg alloys. The amount by which the ultimate shear force (USF) declines varies and is summarised in Table 4. the USF is dependent on the type of cycle as well as component size. The differences between SnAgCu and SnAg are not statistically significant according to the separate variance t-test for differences in two means, with one exception. That is for the R1206 component with cycle F between 0 and 300 cycles. These tables are reproduced graphically in Figures 17, 18 and 19.

The thermal cycle regimes for this work were specifically chosen so that the effect of temperature range, ramp and dwell could be assessed. Cycles A, B and F have the same temperature range (-55 to 125^{o}C) but different ramps and dwells. These results support the trend that ramp rates above 10°C/min cause less damage per cycle, and that increasing the dwell time is not notably damaging. Normally, longer dwells are considered to cause more damage as they allow the solder to stress relax to a greater extent [Ref 4]. That is the ramps and not the dwells that is where the damage occurs is supported by modelling work elsewhere [Ref 9]. The results for R0603 components are similar for cycles A and F, however the change in the USS values is small and therefore less significant.

Comparison of cycles A and C indicates the effect of reducing the minimum temperature of the cycle. Both these cycles have the same upper temperature, ramp and dwell, but cycle C has a minimum temperature of -20^{o}C compared to the -55^{o}C of the A cycle. The lower temperature again causes greater damage as might be expected. A similar but lesser effect can be seen in comparing cycles D and F, both of which have rapid ramps. Cycle F has a lower minimum temperature, -55^{o}C, compared to the -12^{o}C of cycle D with cycle F showing slightly increased damage for all components. The

Comparison of cycles C and E shows the effect of increasing the upper temperature whilst keeping ramp and dwell constant. The upper temperature is 55^{o}C higher for cycle A and the level of damage inflicted is significantly higher for all three component types.

The assessment of thermal cycling loading regimes has shown that slow ramp is causing more damage than longer dwell time (comparing A-B), dwelling at high temperature dwell is causing more damage than dwelling at low temperature (comparing C-E), Liquid-Liquid “thermal shocking”, cycle D, is less damaging per cycle, but overall more effective from a total test time criteria.

The use of thermal shocking can also be compared in terms of the damage caused and the equivalent decrease of USS. Comparing cycling between –20 and 125°C at 10ºC/min with 5 min dwells, cycle C, with the same number of expensive thermal-shocking cycling between –55 and 125°C with rapid ramps of 65°C/min, cycle F, there is a similar decrease in USS. The advantage in using thermal shock regimes is in achieving the solder joint damage about 6 times faster, which in absolute units means thermal-shocking in 5.5 days versus thermal cycling in 33.3 days.

Overall most damage was caused by A cycle which can be recommended for its availability in electronics industry.

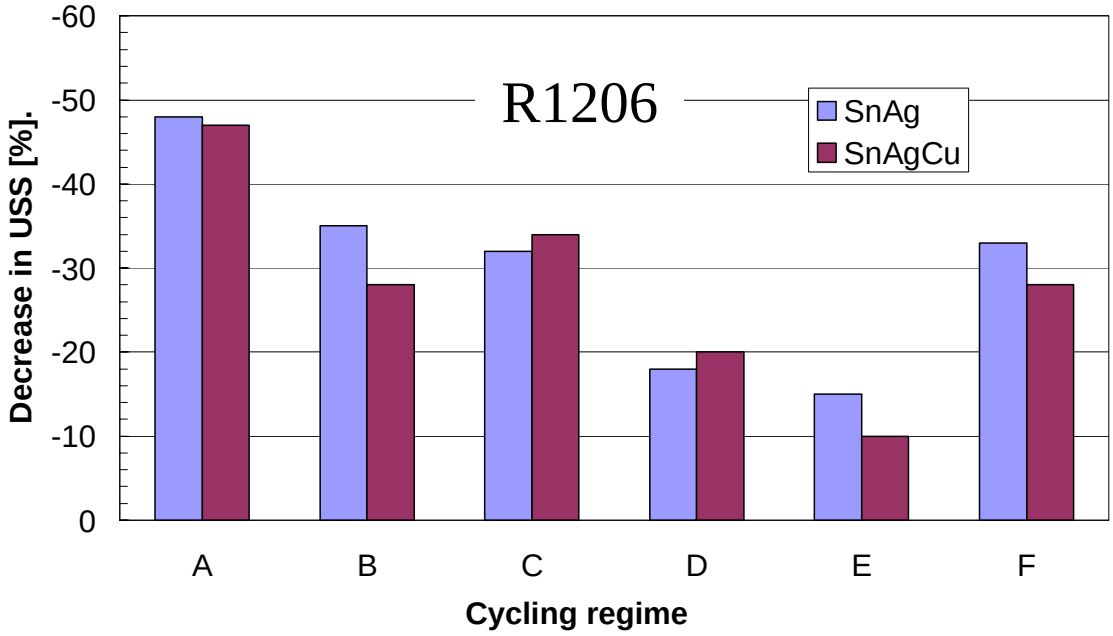

Figure 17 Relative decrease of USS in % after 1200 cycles for 1206 resistors

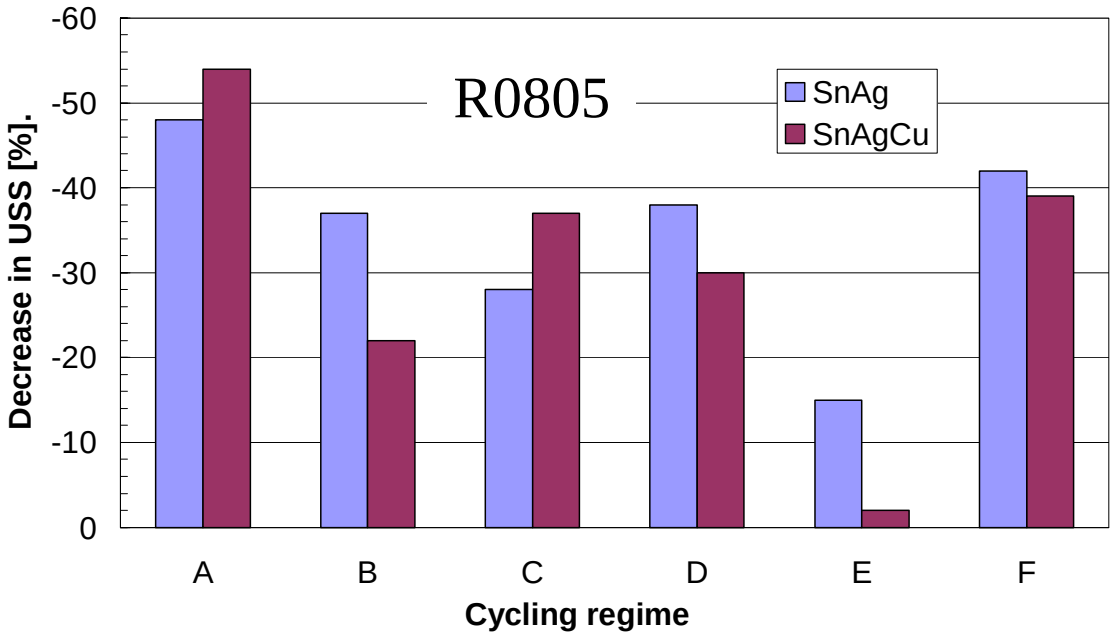

Figure 18 Relative decrease of USS in % after 1200 cycles for 0805 resistors

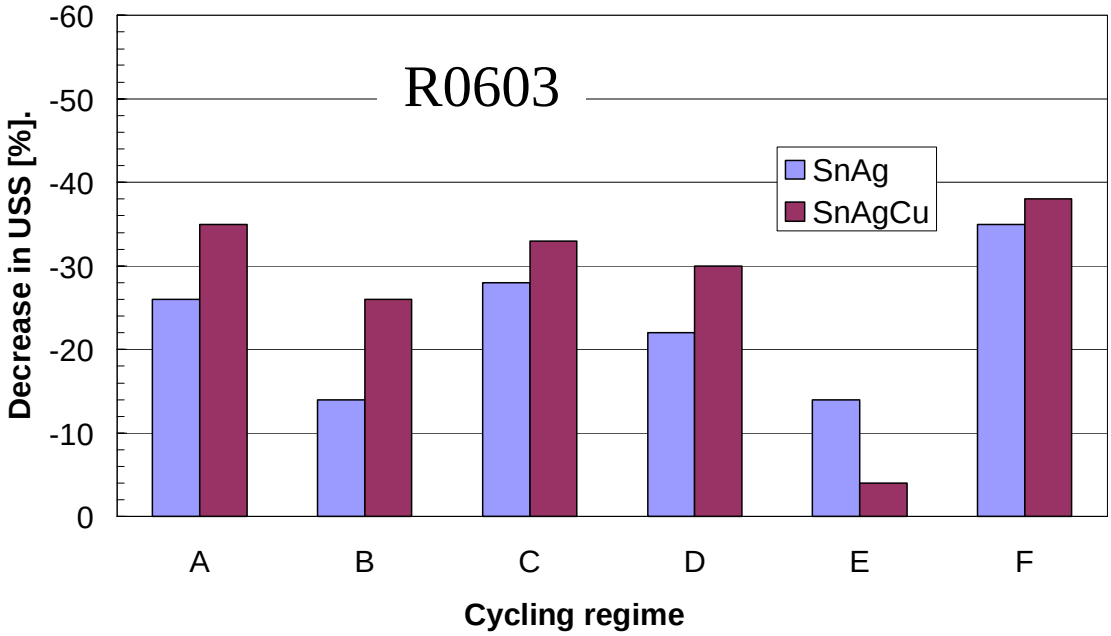

Figure 19 Relative decrease of USS in % after 1200 cycles for 0603 resistors

Increasing the cycling rate to thermal shocking may introduce different failure mechanisms, and hence using thermal shock data may not be invalid. From the data presented here there does not appear to be any anomalous behaviour. Damage decreases per cycle as the ramp rate increases, which is probably due to a reduction in fatigue, but otherwise the behaviour appears similar and using the thermal shocking would not be obviously discounted. A method to establish whether a difference in failure exists between the two cycling rates is to establish the crack path.

Scanning electron microscope analysis of samples from each thermal cycle regime, indicates subtly different failure modes are occurring in those samples which have been subjected to thermal cycle regimes with high ramp rates.

Figures 20, 21 and 22 show fatigue cracks in samples that have undergone slower ramps (<20°C/min). These cracks run through the lower section of the joint under the component and then propagate away from the component termination towards the outside of the solder fillet. Crack propagation in this manner may be most influenced by the TCE mismatch between the component and the substrate.

Figures 23 and 24 show fatigue cracks in samples that have undergone thermal shock testing (>50°C/min). In these samples the fatigue cracks run much closer to the component termination underneath the chip and remain closer to the component termination as they propagate upwards through the solder fillet. Crack propagation in this manner will be more sensitive to TCE mismatch between the component and the solder.

These possible crack propagation routes are shown diagrammatically in Figure 25.

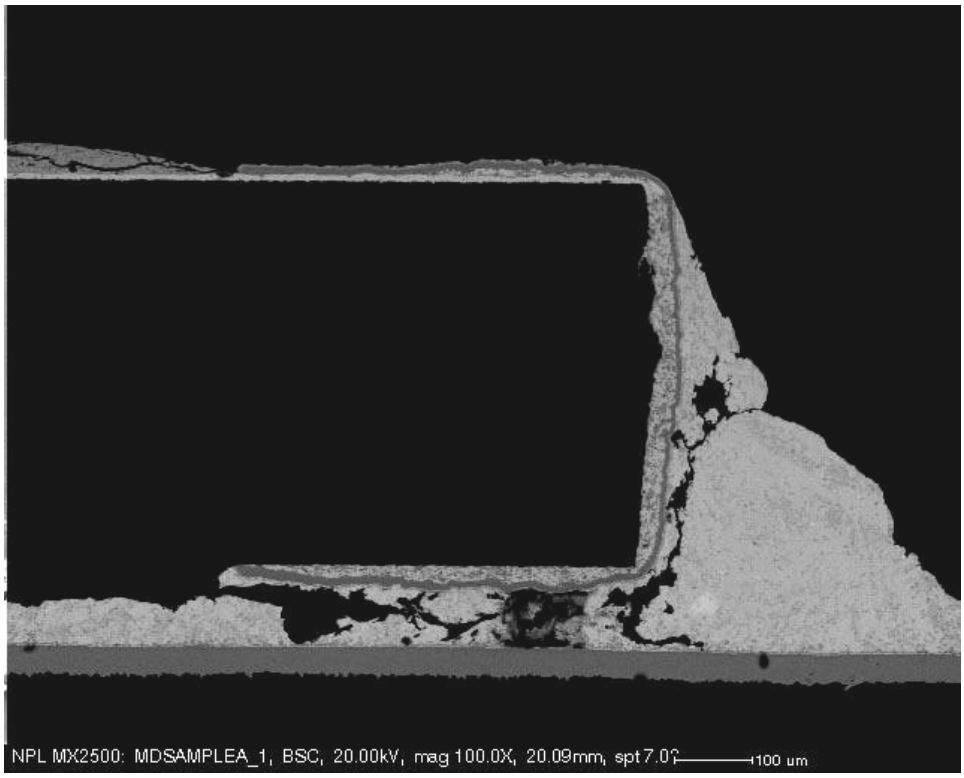

Figure 20: SEM Image of cracked joint of 1200 cycles of thermal cycle A (-55 to 125degC, 10deg/min ramp rate)

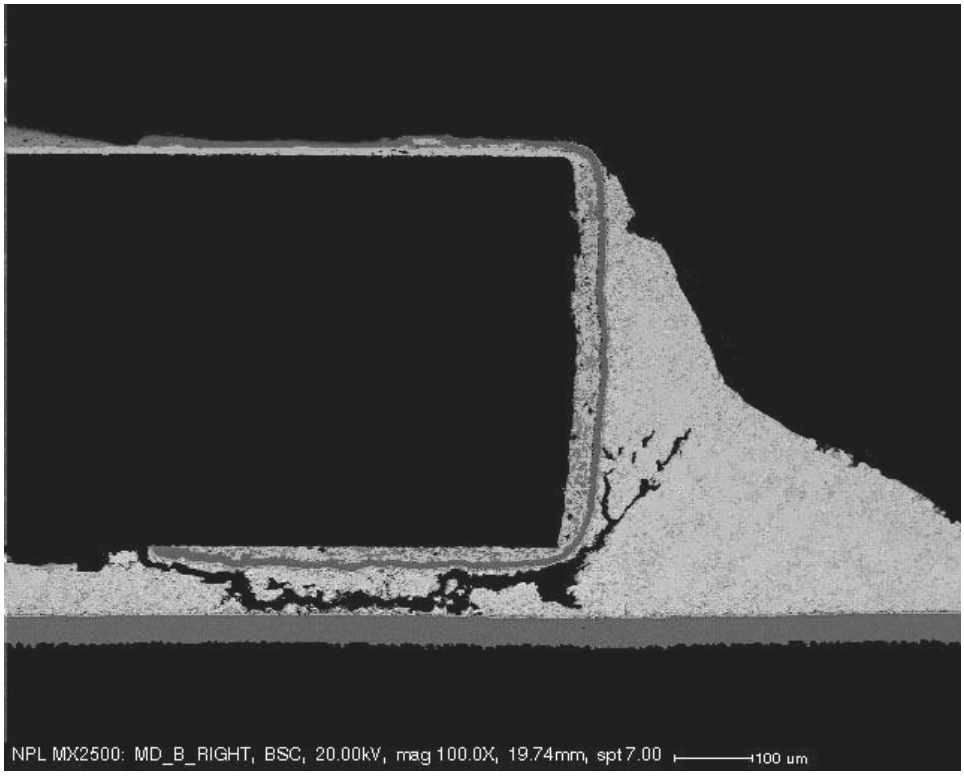

Figure 21: SEM Image of cracked joint of 1200 cycles of thermal cycle B (-55 to 125degC, 18deg/min ramp rate)

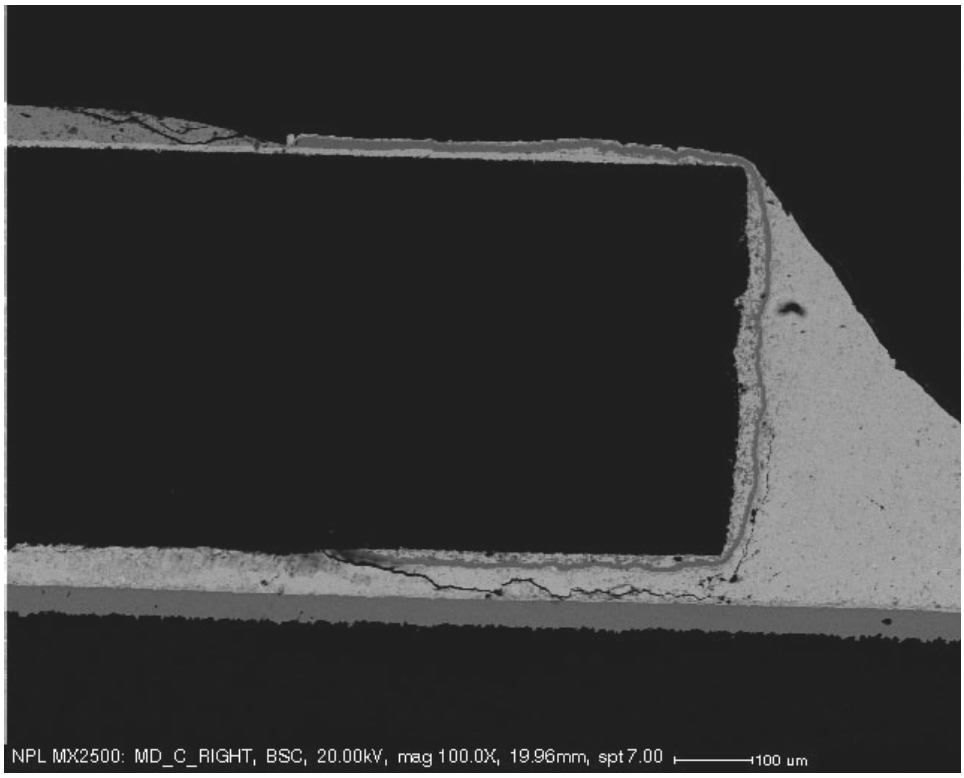

Figure 22: SEM Image of cracked joint of 1200 cycles of thermal cycle C (-20 to 125degC, 18deg/min ramp rate)

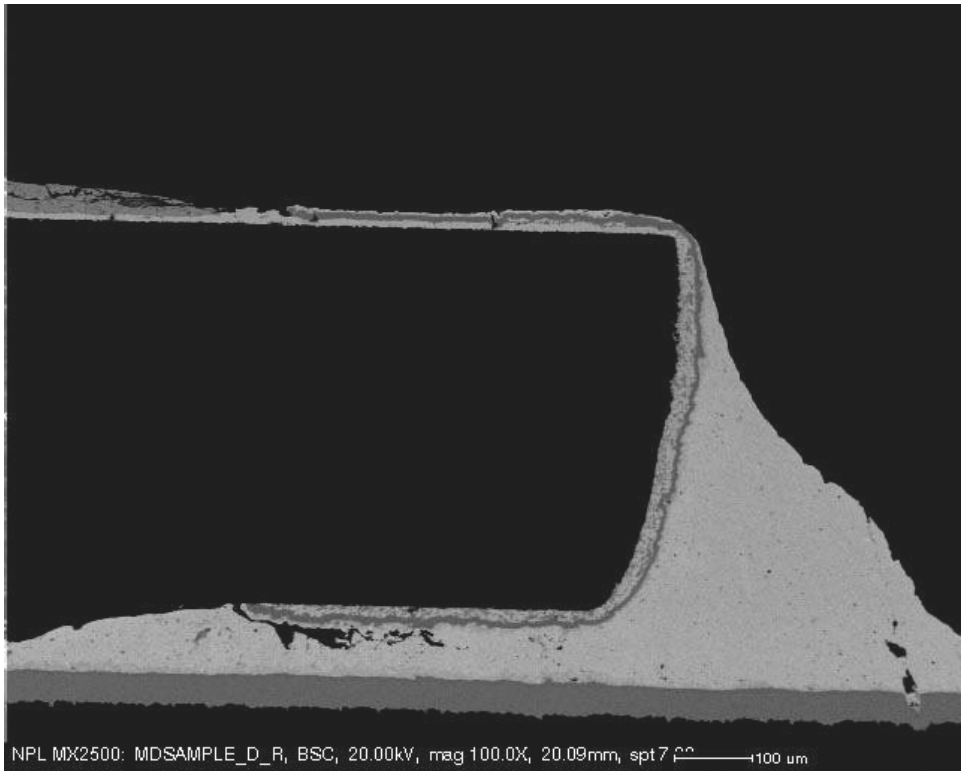

Figure 23: SEM Image of cracked joint of 1200 cycles of thermal cycle D (-12 to 125degC, 65deg/min ramp rate)

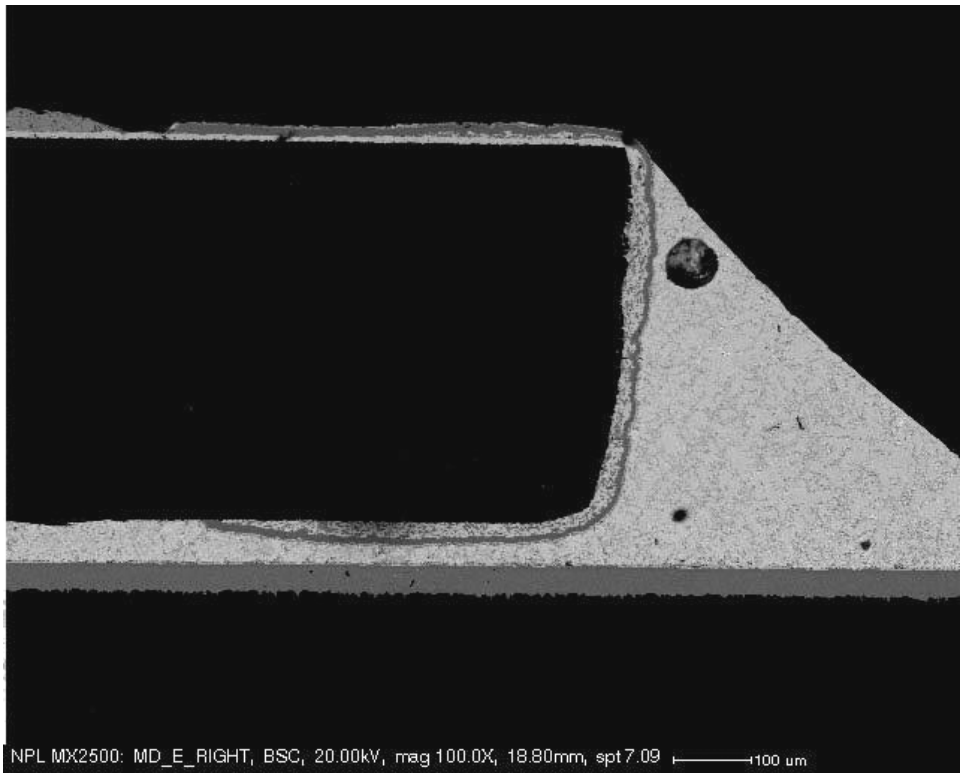

Figure 24: SEM Image of cracked joint of 1200 cycles of thermal cycle E (-20 to 80degC, 10deg/min ramp rate)

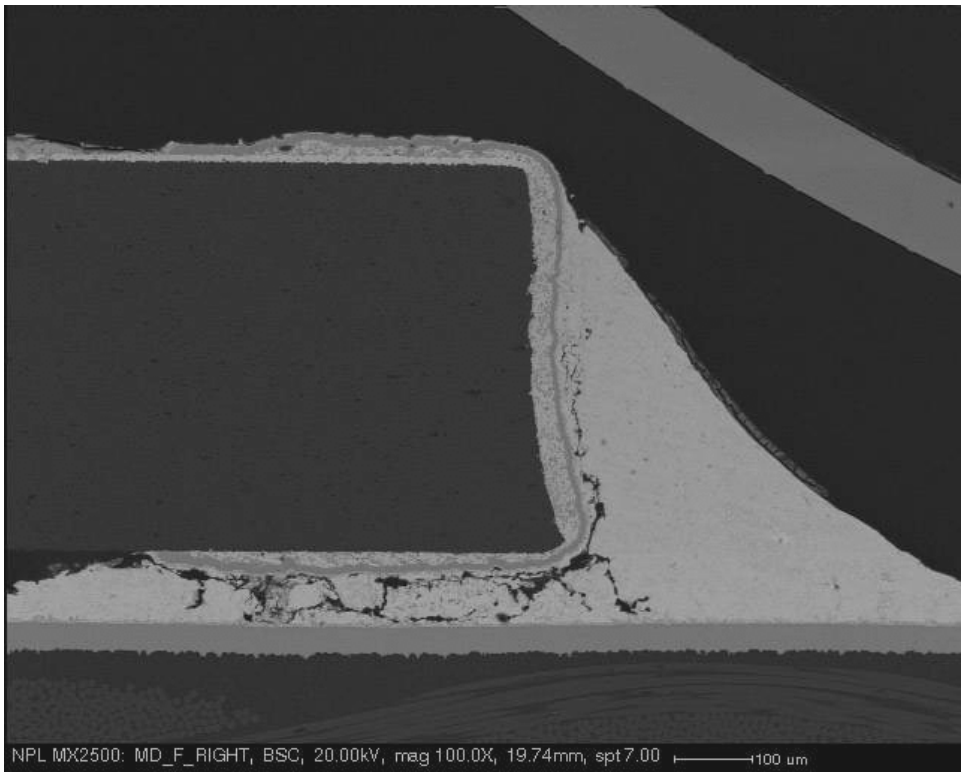

Figure 25 : SEM Image of cracked joint of 1200 cycles of thermal cycle F (-55 to 125degC, 55deg/min ramp rate)

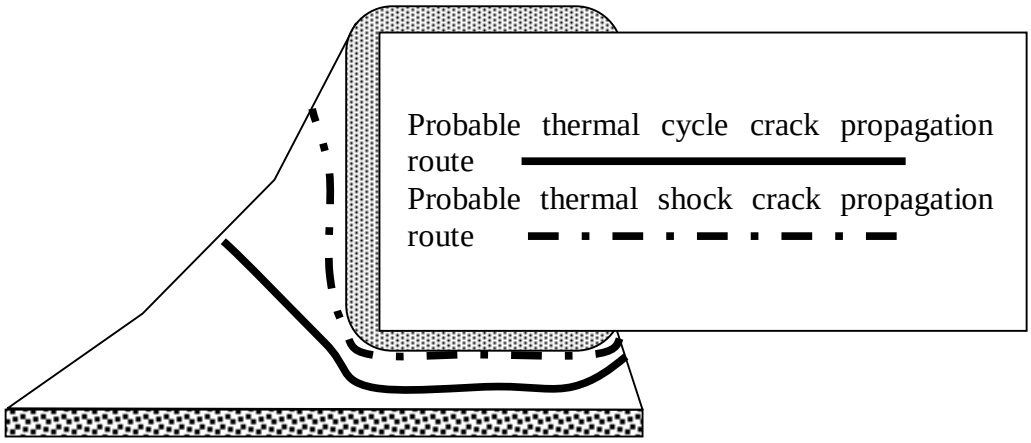

Figure 26 : Probable crack propagation routes

In Figure 25 the tendency for the crack not to follow the same path is shown, and this is a worrying difference. However, the crack does still run through the solder and not some other part of the assembly, such as the component. Hence thermal shocking is stressing the solder, and is therefore critically dependent on the solder properties. This leads us to conclude that thermal shocking can be used for comparative purposes, but for substantive comparisons thermal cycling conditions should be used that are more similar to the use environment.

5 Conclusions

Comparison of accelerated test regimes for lead-free solders undertaken in this work indicates that the most damage to joints is caused by thermal cycling between -55 and 125^{o}C, with a 10^{o}C/min ramp rate and 5 minute dwells. This regime can be recommended to the electronics industry as a suitable accelerated test regime for Pb-free solders.

Large thermal excursions have been shown to give faster results without compromising failure mode. Increasing the upper cycling temperature and reducing the lower temperature both have the effect of increasing fatigue damage. The work has shown that slow ramps cause greater damage than longer dwell times.

Similar degrees of damage were experienced with thermal shock regimes with ramp rates in excess of 50^{o}C/min. However, these latter regimes, although faster to undertake, appear to cause subtly different crack propagation modes than the thermal cycling, with the crack running closer to the component termination. This type of testing may be influenced more by the thermal expansion mismatch between component and solder rather than the mismatch between component and substrate as in the case of the thermal cycling with slower ramps. Thermal shock testing gives quick results (up to 6 times faster due to the increased ramp rates and reduced dwell times) but the failure modes generated may be different to that experienced in field failures. However, the difference may be small and thermal shock testing may be sufficient to differentiate between or enable ranking of process or material changes.

However, due to these small differences in crack propagation modes, thermal cycling should be used to give more representative absolute values or where the difference in expansion rates of the solder and component are high, such as is the case with NiFe lead-frame materials.

The results across all types of cycles showed very little difference in rates of joint degradation between SAC (95.5Sn3.8Ag0.7Cu) and SnAg (96.5Sn3.5Ag) solder alloys.

6 References

1. Clech, J.P. : NEMI report 2003
2. James Oliver, Margareta Nylen, Olivier Rod & Christofer Markou, SIMR : Fatigue properties of Sn3.5Ag0.7Cu solder joints and effects of Pb-contamination : Apex 2003
3. Karl Seelig & David Suraski, AIM : Lead-free electronics assembly for the real world: Joint failures, lead contamination and other important considerations : Apex 2002 additional paper (Partly available on AIM web-site)
4. IPC SM 785 : Guidelines for accelerated reliability testing of surface mount solder attachments. November 1992.
5. Vincent J. : Improved design life and environmentally aware manufacturing of electronics assemblies by lead-free soldering "IDEALS”. Synthesis report BE95-1994

6. Dusek M & Hunt C.P. : Best practice guide for thermal cycling and reliability assessment of solder joints. NPL Report CMMT(A)274. July 2000
7. Dusek M, Nottay J & Hunt CP.. : Compatibility of Lead-free Solders with PCB Materials. NPL Report MATC (A) 89 August 2001
8. Dusek M, Nottay J & Hunt C.P. : The use of shear testing and thermal cycling for the assessment of solder joint reliability. NPL Report CMMT(A)268. June 2000
9. Dusek M & Hunt C.P. : Analytical Model for Thermal-cycling, NPL Report MATC(A)163, March 2004

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