

A Test Methodology for Assessing Pb-free Solder Joint Reliability

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ABSTRACT

This report presents three methods, which together present a test methodology for assessing solder joint reliability. This is based on microsectioning, shear strength and electrical continuity measurements after short-term thermal cycling. The technique of microsectioning, shear testing and continuity measurements are considered to be complementary. The shear testing technique does provide a useful prediction of failure before complete electrical failure occurs. The continuity testing method has an advantage in that large numbers of measurements are involved, providing data that are statistically secure, and since the technique is not destructive the same part can be repeatedly interrogated. Microsectioning is very useful in understanding how the microstructure responds to the applied stress, and in characterising the solder. The recommended guidelines developed here are particularly applicable for chip termination solder joints and BGA solder joints.

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Approved on behalf of Managing Director, NPL, by Dr C Lea,
Head, Centre for Materials Measurement and Technology

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1 INTRODUCTION

The use of shear testing to evaluate accelerated thermocycling is a method that has recently been used for reliability assessment and lifetime prediction [1]. Thermal cycling accelerates the development of cracks and structural changes that will weaken a solder joint. This method is based on the assumption that solder joint strength reduces as the cracks and structural changes develop. The measurement of the solder joint strength will therefore be a function of this microstructural damage. Since electronics assemblies are manufactured from various materials with different thermal coefficients of expansion (TCE), shear strains are placed on the various components in the assembly as it is taken through a thermal cycle. This is shown schematically in Figure 1. Temperature cycling during service induces stresses due to the TCE differences between the mounted component and base substrate, and it is a function of the materials used in electronic assemblies that this strain is relieved in the solder joint. The strain is relieved by microstructural changes and the development of cracks, which accumulate as a consequence of continual cycling.

A conventional method for assessing reliability is to use electrical continuity measurements. Although this method provides a technique in which a large number of joints can be monitored, it is dependent on a complete electrical open circuit occurring before any failure is registered. This can be a severe handicap when over 5000 cycles may be required to reach a failure. To reduce the experimental time in assessing a solder alloys, components are selected which are known to be more prone to solder joint failure, and are often referred to as “weak links”. Typically with these components the TCE mismatch is high, and in this study we have used 2512-type ceramic resistors and large BGAs. These “weak link” components are the most likely to suffer solder joint failure on commercial products.

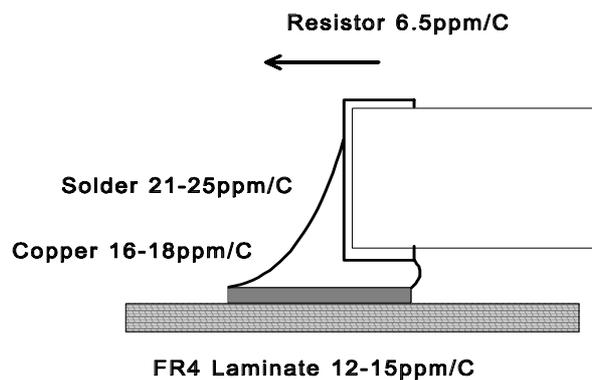


Figure 1. TCE (X-axis) mismatches in SM assemblies

2 ACCELERATED THERMOCYCLING

There are many temperature profiles currently in use today. OEMs have developed their own temperature profiles that are relevant to their products. Some typical industry temperature cycles are listed in Table 1 with a schematic shown in Figure 2, in which the dwells are labelled as T1 and T2 and are usually equal in length, with the idealised linear ramps between the two set points.

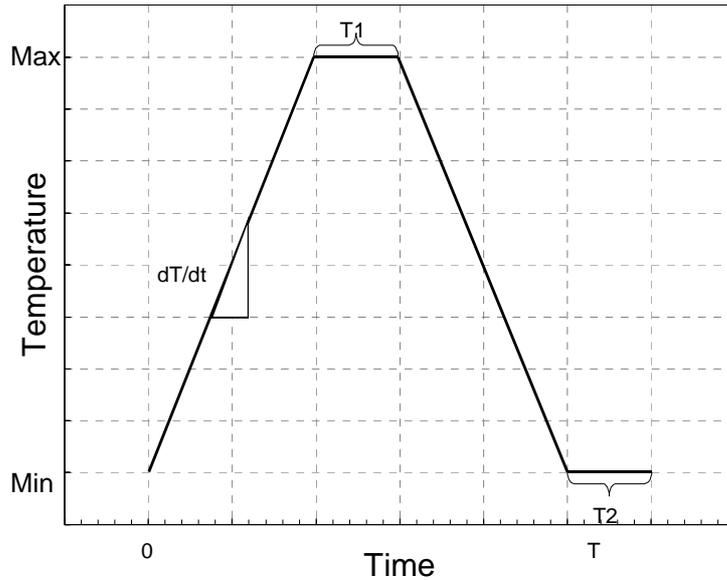


Figure 2. Temperature cycle definition

Table 1. Selection of temperature cycles used in industry

Category	T max [°C]	T min [°C]	~T [min]	T1≡T2 [min]	dT/dt [°C/min]
Automotive under hood and Military	+125	-55	48	15	20
Military Avionics	+95	-55	45	15	20
Telecom	+85	-40	43	15	20
Consumer electronics	+60	0	36	15	20

The most common profile is that based around the military and automotive applications in the first row of Table 1. Figure 3 reproduces an example of a real temperature cycle used for evaluating thermal-mechanical fatigue of solder joints in a recent NPL study measured on a

tested part. The two set temperatures points are: $-55\text{ }^{\circ}\text{C}$ and $+125\text{ }^{\circ}\text{C}$ with 5 minutes dwells. The 5 min dwell is defined as the time during which the temperature in a thermocycling oven was within $\pm 5\text{ }^{\circ}\text{C}$ of the set value.

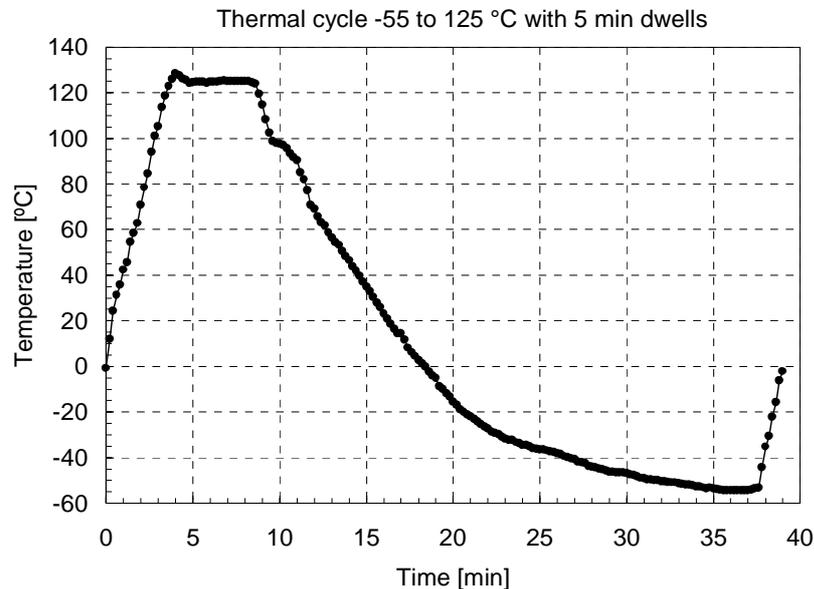


Figure 3. Example of a temperature cycle

3 COMPONENT PREPARATION

Any evaluation must use representative parts of the assembly with respect to the material TCE differences. Some attention should be paid to the components used to evaluate the assembly, the so-called “*weak links*”. Chip resistors are an ideal choice, since their rigid alumina bodies have a significantly different TCE from the pcb base material (FR4), and hence are more prone to fail from stress accumulation in the solder joints. The other advantage of using SM chip resistors as testing devices is the simplicity of joint failure detection. High resistance, or open circuit, is easily recognised using direct current (DC) measurement. Another type of *weak link* SM solder joint is the BGA solder bump, although this is dependent on component design. If there is a need to test solder materials that are unavailable in BGA-bump version (i.e. lead-free solders), the BGA components should be reballed at the time of board assembly. The recommended re-balling procedure should incorporate these steps:

- 1) **De-balling BGA:** wicking of original solder bumps with a fluxed Cu braze.
- 2) **Cleaning BGA:** cleaning the package can be cleaned with IPA to remove flux residues and provide a flat surface suitable for printing operations.
- 3) **First print at building balls:** pointing the first layer of corresponding solder paste on a BGA package, using $150\text{ }\mu\text{m}$ stainless steel stencils.
- 4) **Reflow:** reflowing of first print into bumps.
- 5) **Second print at building balls:** printing a second layer of solder paste on the first layer of bumps. The first layer of bumps significantly helps alignments of component and stencil.

- 6) **Reflow:** reflowing the first layer of bumps and second printed layer, building the bump volume.
- 7) **Printing and Reflow:** applying third and fourth layers, following the print and reflow operation described above to increase the solder bump volume (Figures 4 and 5).
- 8) **Storage:** protecting re-balled package from ambient humidity before final PCB reflow operation

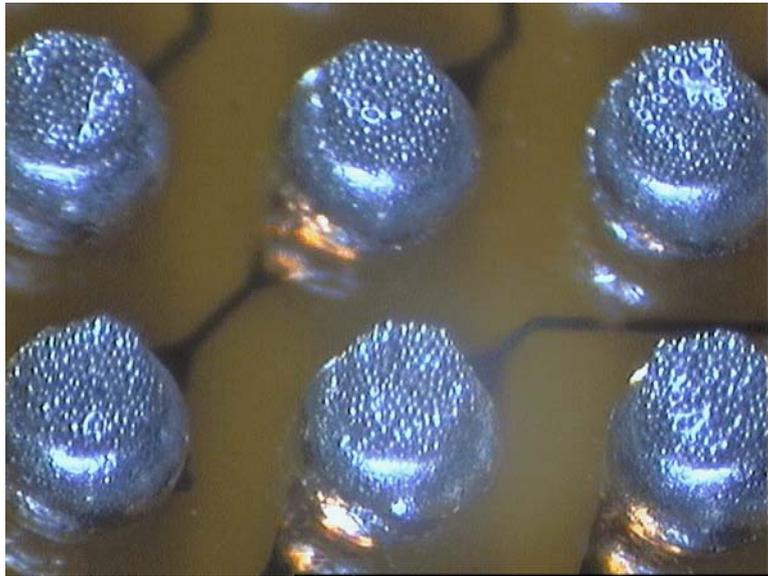


Figure 4. Re-balling of BGAs



Figure 5. Re-balling of BGAs following a print stage, side view

An example of a dedicated pcb layout for reliability testing is shown in Figure 6. The pcb is a single sided 1.6 mm thick FR4 board with 35 μm thick Cu tracks. The design incorporates 20 off 0805-type resistors, 20 off 2512-type resistors, four PBGAs and 12 SOICs. The resistors and PBGAs have circuitry to the connectors for continuity measurements.

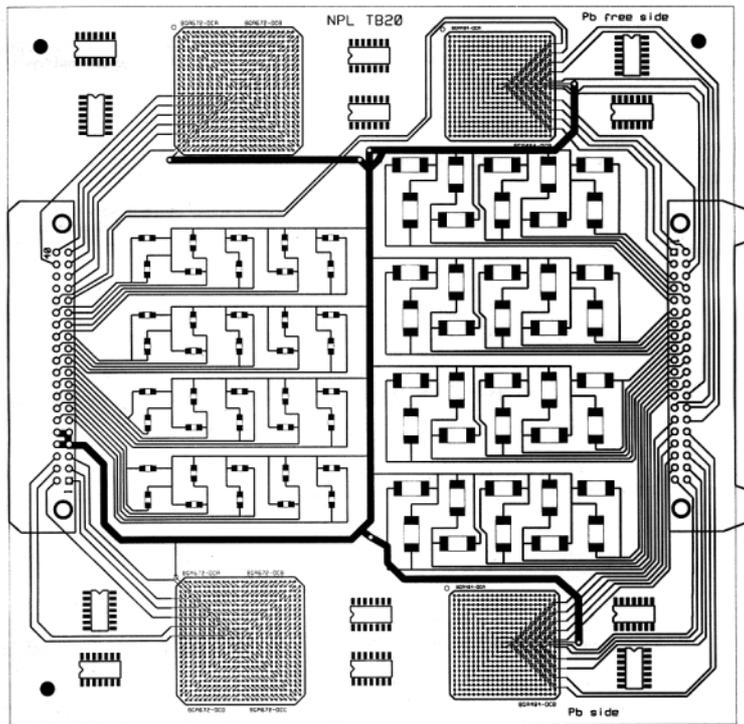


Figure 6. Example of test PCB layout, size 152 x 152 x 1.6 mm

4 FAILURE EVALUATION

4.1 MICROSECTIONING

4.1.1 Specimen Preparation

Samples should be cut from test boards using a conventional diamond saw that is liquid cooled. This method of cutting ensures that soldered joints do not overheat to a level that would affect the microstructure. The cut samples should be cleaned using conventional IPA (iso-propyl alcohol) to ensure complete removal of any residue left from the cutting stage. A suitable resin should be selected for sample mounting that gives excellent fill and preserves the sample edges and does not exceed 80°C during curing. Cold curing epoxy resins are a suitable choice.

It is important to note that any process, whether cutting or mounting, should not involve elevated temperatures. The latter can cause changes in the microstructure such as precipitation of a second phase from a supersaturated solid solution or solid-state diffusion reactions between the tin present within the solder and the copper pads present on the board.

4.1.2 Metallography

Samples should be ground with successive grades of silicon carbide of 120 to 4000 grit papers, followed by polishing with diamond pastes/sprays with successive particle sizes from 15 to 0.25 µm in diameter. Care must be taken to ensure that only a light pressure is used, due to the relative differences in the hardness of the solder, to the copper pad, any interlayer present, and the component edge. Diamond impregnation of the polishing cloth needs to be kept to a maximum to ensure an optimum cutting rate. Final polishing of the samples should be carried out by hand using a gamma aluminate powder suspended in lapping fluid.

If etching of the samples is required, for example to highlight microstructure, the following procedures should be used:

Lead based solders: use a solution containing 2 ml hydrochloric acid and 98 ml industrial methylated spirits in a polish-etch technique employing 0.25µm diamond paste as the polishing medium.

Lead-free solders: use 2 ml nitric acid, 2 ml hydrochloric acid and 96 ml distilled water in a polish-etch technique with 0.25µm diamond paste as the polishing medium.

It is recommended that micrographs of the microstructure in the range of 100 to 500 magnification should be generated and filed.

4.2 SHEAR TESTING

4.2.1 Specimen Preparation

The boards used for shear strength testing should be cut to size so that they fit within the shear testing instrument. Ideally a sample may contain two or three components for testing. The boards should be cut with a conventional water-cooled diamond saw, so as to introduce as little

stress as possible into the board. The cut boards should be cleaned to remove any contaminants/residues from the cutting process and dried using compressed air.

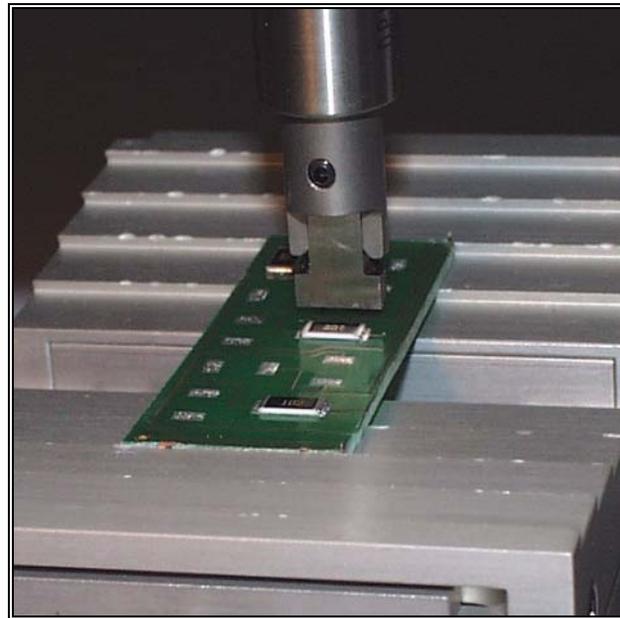


Figure 7. Shear test jig and push-off tool.

Figure 7 shows a possible experimental arrangement of a board placed within a jig ready for testing. As the jig is mounted on a movable X-Y table, this can be re-positioned so that the shear-test tool is directly behind the component (as shown in Figure 7). In this test the push-off tool is used at a pre-set height (centre of component) of $80\ \mu\text{m}$ (for a 2512-type chip resistor) and driven at a defined speed of $200\ \mu\text{m/s}$. The end of a typical test is shown in Figure 8.

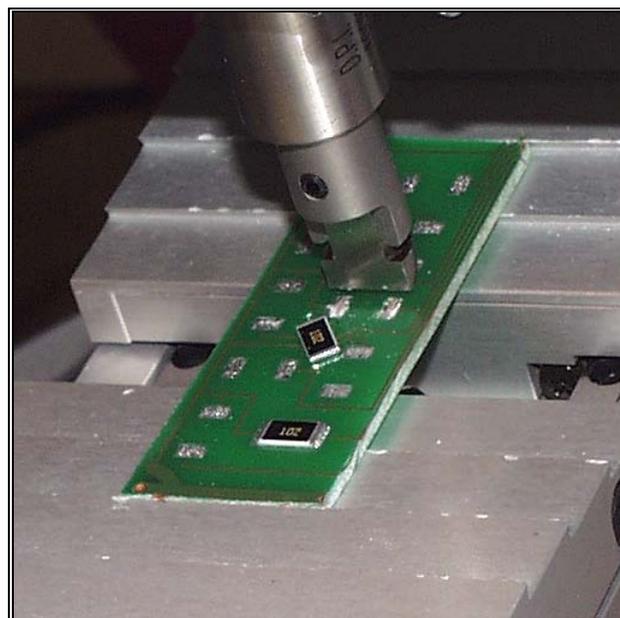


Figure 8. Typical joint break after failure.

For each thermally cycled board at least 10 resistors need to be tested in order to produce a meaningful accurate statistical average of joint strength.

4.3 Electrical Continuity Measurements

To detect an electrical failure, two basic systems can be used: static or periodic, and dynamic monitoring. The periodic approach entails monitoring of electrical continuity of test samples off-line, i.e. removed from thermocycling chamber and at room temperature. For dynamic monitoring of electrical continuity, the samples remain in-situ i.e. in the thermocycling chamber during thermal excursions, with measurements taken during the temperature ramp and/or at the max and min temperature dwells.

The advantage of static-periodic data lies with the data acquisition. In the periodic mode multiple boards can be tested sequentially using only one connector. Therefore a large number of components can be assessed, and since the connection to the board is made each time a measurement is carried out the electrical contact in the edge connector is generally very reliable. A disadvantage of this method is the precision in detection of the number of cycles to failure. Clearly not measuring in-situ failure means that events can be missed, particularly those occurring at the extreme temperatures of the high and low dwells.

The advantage of dynamic monitoring is the high probability of capturing a failure. The limitations of this approach relate to the monitoring capacity, which is restricted by the number of channels on the multiplexer. Another significant issue is the viability of the board connections with the test chamber, which are also exposed to the thermal cycling regime. The connector robustness is a key issue for accurate measurement.

An advanced and expensive type of dynamic testing equipment is that used in the telecommunications industry, namely an event detector. This works as a dynamic monitoring apparatus with an in-line processing control unit detecting a real time failure with a response time of a few milliseconds.

Components suitable for continuity testing such as chip resistors and BGAs should be electrically tested prior to thermal cycling and then periodically measured after a fixed number of cycles ~ 50-200. The resistance of a tested component can be measured by the Voltage Method, in which a constant voltage is applied across a device and the current through the device measured. Figure 9 presents a schematic diagram of the measurement circuitry.

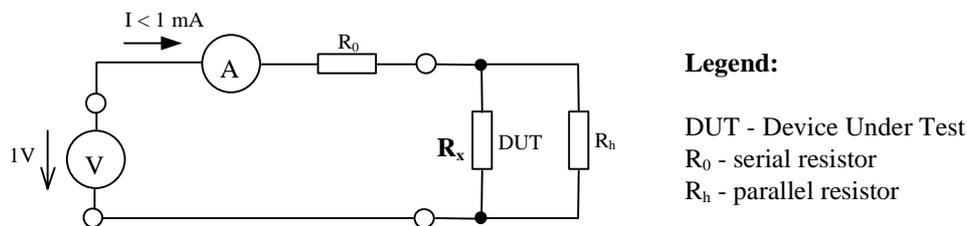


Figure 9. Schematic circuit of the measurement method

An example of static-periodic monitoring based on Voltage source Measure Unit (Keithley) is outlined below.

The component to be tested (DUT), daisy chained if necessary, is connected into a simple circuit with a voltage source (1V) and amp meter so that the resistance can be calculated. The nominal current should be below 1 mA; a higher current will melt partial fractured solder joints [4]. To limit the current, a resistor R_0 is used. To restrict the time of measurement (integration time of meter), resistor R_h (1 M Ω , or greater, is recommended) is connected in parallel across the measured device (DUT).

As the tested components are periodically measured for failure detection, the pass/fail criterion can be defined for R_x , e.g. 10 % above nominal value of the resistance. A test board should be designed to allow multiple testing of samples, which can be connected through a connector and switch bridge device. An example of measurement apparatus is shown in Figure 10. From the failure analysis a Weibull distribution can be fitted to the failure rate, and the N_f median numbers of cycles for 50 % failure rate can therefore be estimated [6]. The error of this measurement depends on the probability of a failure detection [4] and the sampling rate of continuity measurements.

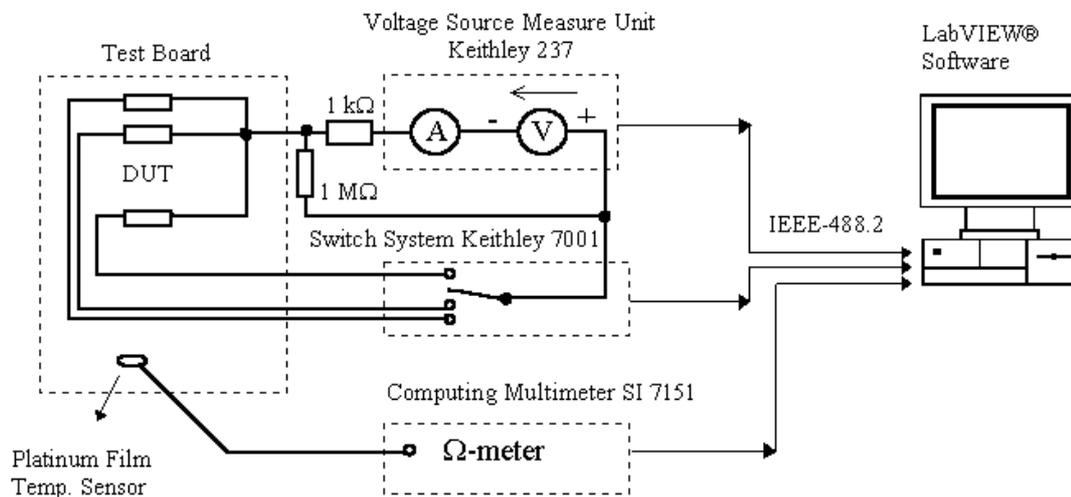


Figure 10. An example of continuity testing apparatus

5 CONCLUSION

Three methods are discussed for evaluating the performance of solder joints in a thermocycling experiment in which the thermo-mechanical fatigue properties of solders are evaluated. The technique of microsectioning, shear testing and continuity measurements are considered to be complementary. The shear testing technique does provide a useful prediction of failure before complete electrical failure occurs. The continuity testing method has an advantage in that large numbers of measurements are involved, providing data which are statistically secure, and since the technique is not destructive the same part can be repeatedly interrogated. Microsectioning is very useful in understanding how the microstructure responds to the applied stress, and in characterising the solder.

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